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Re Applic of	David C. Long, et al.
Docket No.	FIS920010163US1
Serial No.	10/016,090
Filing Date	12/13/01
Attorney	Ira D. Blecker

Attached: Appeal Brief, Transmittal of Appeal Brief

PLEASE DELIVER TO:
EXAMINER: Poker, Jennifer A.
ART UNIT: 2832
PHONE NO:
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TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. FIS920010163US1

In Re Application Of: David C. Long, et al.

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/016,090	12/13/01	Poker, Jennifer A.	32074	2832	6883

Invention: EMBEDDED INDUCTOR AND METHOD OF MAKING

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on 1/24/05

The fee for filing this Appeal Brief is: $500.00

☐ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

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Ira D Blecker
Signature

Dated: Feb. 24, 2005

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Patent
IBM Docket No. FIS920010163US1

10/016,090

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Date: 2/24/05

In re Application of: David C. Long, et al. **Filed:** 12/13/01

For: EMBEDDED INDUCTOR AND METHOD OF MAKING

Serial Number: 10/016,090 *CONFIRMATION NO.*: 6883

Art Unit: 2832 *Examiner:* Poker, Jennifer A.

APPEAL BRIEF

Hon. Commissioner of Patents and Trademarks
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

On January 24, 2005, Appellants appealed to the Board of Patent Appeals and Interferences from the decision of the Primary Examiner finally rejecting claims 1, 2, 4 to 13 and 21 to 23. What follows is Appellants Appeal Brief as required by 37 CFR 41.37.

REAL PARTY IN INTEREST:

International Business Machines Corporation, the assignee of the entire interest of the present application, is the real party in interest in this appeal.

RELATED APPEALS AND INTERFERENCES:

There are no related appeals and interferences.

STATUS OF CLAIMS:

Claims 1, 2, 4 to 13 and 21 to 23 are pending in this appeal and all of claims 1, 2, 4 to 13 and 21 to 23 have been finally rejected by the Examiner. Claims 3 and 14 to 20 have been canceled. No claims are allowed.

STATUS OF AMENDMENTS:

An Amendment After Final Rejection was filed November 23, 2004. In an Advisory Action mailed January 26, 2005, the Examiner did not allow the application and, further, for purposes of appeal, the Examiner indicated that the Amendment After Final Rejection will not be entered. Subsequent to the Advisory Action, however, the undersigned on February 7, 2005, spoke with Examiner Poker who advised the undersigned that she did a Supplementary Advisory Action (which because of Office delays has yet to be mailed to Appellants) in which Appellants' Amendment After Final Rejection will be entered. Having not received the Supplementary Advisory Action, the undersigned again spoke with Examiner Poker on February 16, 2005, and Examiner Poker advised the undersigned that she had spoken with her Supervisory Patent Examiner and that the Amendment After Final Rejection will, in fact, be entered. The claims presented in the Claims Appendix are as presented in the Amendment After Final Rejection.

SUMMARY OF CLAIMED SUBJECT MATTER:

The present invention pertains to an inductor which is buried or embedded in a dielectric substrate. The dielectric substrate is preferably a multilayer ceramic (MLC) substrate although other materials, such as organic materials, are not excluded. Q is a quality factor for inductors and is

defined as the ratio of its reactance to its effective series resistance at a given frequency. It would be desirable to have an embedded inductor with a relatively high Q value and high inductance.

Figure 1 illustrates an embedded inductor 12 in a dielectric substrate 10. The layers of the dielectric material that would normally surround the embedded inductor 12 have been removed for clarity. Figure 9 is a cross section of the embedded inductor 12 with the various dielectric layers in place. Returning to Figure 1, each turn of the embedded inductor 12 includes a bottom portion 20, a top portion 18 and two side portions 22. The top portion 18 and bottom portion 20 are parallel but in different layers. As shown in Figure 1, bottom portion 20 is in a first layer while top portion 18 is in another layer several layers away. The side portions 22 are parallel to each other. The top portions 18 and bottom portions 20 are formed by screened lines while side portions 22 comprise vias so that the top portions 18 and side portions 20 have lower crossectional area than the side portions 22. (Specification page 9, lines 13-23 to page 10, lines 1-10).

However, because the top portions 18 and side portions 20 have lower crossectional area than the side portions 22, they create higher resistance. Structural changes which minimize the resistance of the top portions 18 and bottom portions 20 create higher Q values. (Specification, page 11, lines 18-24).

Figures 3 to 5 (claim 1) and Figure 5 (claim 23) illustrate preferred embodiments of the invention in which structural changes have been made to the top portions 18 and bottom portions 20 to achieve

both high Q value and high inductance.

For the convenience of the Board, claim 1 claiming a first preferred embodiment of the invention is reproduced here as follows:

1. A dielectric substrate having a multiturn inductor comprising:

a) a multilayer dielectric body comprising a plurality of layers;

b) a multiturn inductor buried within the dielectric body, each turn of the inductor comprising a bottom portion, a top portion and two side portions, the bottom portion and top portion being parallel and in different layers of the dielectric body, the side portions being parallel to each other and extending between the top and bottom portions and comprising vias in the dielectric body, wherein the top and bottom portions have a lower crossectional area than the side portions and wherein the top and bottom portions each comprise two parallel wiring lines in juxtaposition.

Referring to Figures 3 and 4, the embedded inductors 112, 212 are shown wherein the top portion 18 comprises top subportions 18A and 18B and bottom portion 20 comprises bottom subportions 20A and 20B. (Specification, page 12, lines 1-6). The top subportions 18A and 18B are one over the other but separated by one layer while bottom subportions 20A and 20B are likewise one over the other separated by one layer. Embedded inductors 112, 212 are similar to embedded inductor 12 shown in Figure 1 except for the top subportions 18A and 18B and botom subportions 20A and 20B. Figure 5 similarly shows the embodiment having separate top subportions and bottom subportions. By increasing the metal in the top portions 18 and bottom portions 20, the resistance of the embedded inductor is reduced, thereby increasing its inductance.

For the convenience of the Board, claim 23 claiming a second preferred embodiment of the invention is reproduced here as follows:

23. A dielectric substrate having a multiturn inductor comprising:

a) a multilayer dielectric body comprising a plurality of layers;

b) a multiturn inductor buried within the dielectric body, each turn of the inductor comprising a bottom portion, a top portion and two side portions, the bottom portion and top portion being parallel and in different layers of the dielectric body, the side portions being parallel to each other and extending between the top and bottom portions and comprising vias in the dielectric body, wherein the top and bottom portions have a lower crossectional area than the side portions and wherein the top and bottom portions each comprise at least two parallel wiring lines of unequal length in juxtaposition.

Referring to Figure 5, the embedded inductor 312 is similar to embedded inductor 12 shown in Figure 1 except that embedded inductor 312 has top subportions and bottom subportions which are unequal in length. According to this embodiment of the invention, the inductor loop has been made closer to circular shape to further increase the Q of the embedded inductor 312. (Specification, page 12, lines 12-14).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL:

I. The §102 rejections:

A. Claims 1 to 6 and 21 to 23 have been rejected by the Examiner under 35 USC §102(e) as being anticipated by Ahn et al. U.S. Patent 6,531,945 (hereafter "Ahn").

II. The §103 rejections:

A. Claim 7 has been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Ahn in view of Burghartz et al. U.S. Patent 5,884,990.

B. Claims 8 to 10 and 13 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Ahn in view of Liu et al. U.S. Patent 6,459,352 (hereafter "Liu").

C. Claims 11 and 12 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Ahn in view of Eberhardt U.S. Patent 5,461,353 (hereafter "Eberhardt").

ARGUMENT:

I. The §102 rejections:

A. Claims 1 to 6 and 21 to 23 have been rejected by the Examiner under 35 USC §102(e) as being anticipated by Ahn et al. U.S. Patent 6,531,945 (hereafter "Ahn").

"Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." W.L. Gore & Assocs. V. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). If any element is missing, the claim is not anticipated. In re Royka and Martin, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

As Appellants will argue, each of claims 1, 4 to 6 and 23 contain elements which have not been disclosed in Ahn, thereby compelling the conclusion that claims 1, 4 to 6 and 23 are not anticipated by Ahn.

(i) Patentability of claim 1:

Claim 1 claims the embodiments as illustrated in Figures 3 to 5. As recited in claim 1, each turn of the inductor comprises a bottom portion, a top portion and two side portions. These embodiments further illustrate, and claim 1 further recites, that the top and bottom portions (of each turn of the inductor) comprise two parallel wiring lines in juxtaposition (...each turn of the inductor comprising a bottom portion, a top portion and two side portions...wherein the top and bottom portions each

comprise two parallel wiring lines in juxtaposition." [emphasis added]). Referring to Figures 3 and 4, it can be seen that top portion 18 of each turn of the inductor comprises two parallel wiring lines 18A, 18B in juxtaposition and bottom portion 20 of each turn of the inductor comprises two parallel wiring lines 20A, 20B in juxtaposition. Figure 5 also illustrates separate top and bottom subportions of each turn of the inductor. Such an arrangement as illustrated in Figures 3 to 5 minimizes the resistance of the top and bottom portions, thereby increasing the inductance and optimizing Q (see specification, page 11, lines 18-24, and page 12, lines 1-6).

Ahn discloses a multilayer dielectric body having an embedded inductor wherein each turn of the inductor includes top and bottom portions 220 and sides (paths) 140. Each turn of the Ahn inductor comprises only a single wiring line for the top portion 220 and a single wiring line 220 for the bottom portion. While Ahn does show top portions and bottom portions in juxtaposition, these are in different turns of the inductor, contrary to the limitations of Applicants' claim 1 which require the juxtaposed parallel wiring lines in each turn of the inductor (...each turn of the inductor comprising a bottom portion, a top portion and two side portions...wherein the top and bottom portions each comprise two parallel wiring lines in juxtaposition." [emphasis added]). As Ahn fails to teach the foregoing limitation of juxtaposed parallel wiring lines in each turn of the inductor, Ahn cannot anticipate Appellants' claim 1.

(ii) Patentability of claim 23:

Claim 23 is similar to claim 1 except that the juxtaposed parallel wiring lines in each turn of the inductor are of unequal length (...wherein the top and bottom portions each comprise at least two parallel wiring lines of unequal length in juxtaposition.). This is the embodiment shown in Appellants' Figure 5. More importantly, the configuration shown in Figure 5 more closely approximates the shape of a circle so as to further increase the Q of the embedded inductor. Ahn does not show the embodiment claimed in claim 23. In the final Office Action, the Examiner states that Ahn illustrates that the top and bottom portions are of unequal length in juxtaposition. This may be true but this is not what is claimed by Appellants. Appellants are claiming that "...the top and bottom portions each comprise at least two parallel wiring lines of unequal length..." [emphasis added]. Since Ahn shows top and bottom portions each comprising only one wiring line, Ahn cannot show top and bottom portions each comprising at least two parallel wiring lines of unequal length. As Ahn fails to show this limitation of Appellants' claim 23, Ahn cannot anticipate Appellants' claim 23.

Inasmuch as claims 2, 4 to 6, 21 and 22 depend from claim 1, and since claim 1 is believed to be patentably distinguishable over Ahn, then claims 2, 4 to 6, 21 and 22 should be patentable as well.

(iii) Patentability of claim 4

In addition, claim 4 is believed to be independently patentable.

Claim 4, which depends from claim 1, claims vias connecting the juxtaposed parallel wiring lines of the top and bottom portions. As noted above, these juxtaposed wiring lines are in each turn of inductor.

Ahn discloses only paths 140 between the top and bottom portions 220 of the inductor. These paths 140 are equivalent to the side portions of Appellants' inductor. However, Ahn can not show vias between the juxtaposed parallel wiring lines of the top and bottom portions of each turn of the inductor because Ahn does not show parallel wiring lines of the top and bottom portions of each turn of the inductor (as explained above with respect to claims 1 and 23) and, in addition, does not show vias between those parallel wiring lines as claimed by Appellants in claim 4.

In the final Office Action, the Examiner states that "The paths (140) can advantageously comprise vias...The vias are filled with conductive posts (210), which connect the ends of the top and bottom portions...". However, it is submitted that the Examiner fails to appreciate that Appellants' claim 4 requires that each of the top and bottom portions recite parallel wiring lines, and vias between those parallel wiring lines, while the top and bottom portions of Ahn only show single wiring lines. It is impossible for Ahn to show vias between parallel wiring lines as claimed by Appellants since Ahn fails to show parallel wiring lines that make up the top and bottom portions of each turn of the inductor and thus Ahn cannot show vias between such nonexistent parallel wiring lines. As Ahn fails to show the limitation of claim 4, Ahn cannot anticipate Appellants' claim 4.

(iv) Patentability of claim 5

Claim 5 is believed to be independently patentable.

Claim 5, which depends from claim 4, claims vias connecting the juxtaposed parallel wiring lines of the top and bottom portions only at the ends of the lines. This feature is shown in Figure 3.

Ahn discloses only paths 140 between the top and bottom portions 220 of the inductor. These paths 140 are equivalent to the side portions of Appellants' inductor. However, Ahn can not show vias only at the ends of and between the juxtaposed parallel wiring lines of the top and bottom portions of each turn of the inductor because Ahn does not show parallel wiring lines of the top and bottom portions of each turn of the inductor (as explained above with respect to claims 1 and 23) and, in addition does not show vias only at the ends and between those parallel wiring lines as claimed by Appellants in claim 5.

In the final Office Action, the Examiner states that "The paths (140) can advantageously comprise vias...The vias are filled with conductive posts (210), which connect the ends of the top and bottom portions...". However, it is submitted that the Examiner fails to appreciate that Appellants' claim 5 requires that each of the top and bottom portions recite parallel wiring lines, and vias at the ends of and between those parallel wiring lines, while the top and bottom portions of Ahn only show single wiring lines. It is impossible for Ahn to show vias between parallel wiring lines as claimed by

Appellants since Ahn fails to show parallel wiring lines that make up the top and bottom portions of each turn of the inductor and thus Ahn cannot show vias at the ends of and between such nonexistent parallel wiring lines. As Ahn fails to show this limitation of claim 5, Ahn cannot anticipate Appellants' claim 5.

(v) Patentability of claim 6

Claim 6 is believed to be independently patentable.

Claim 6, which depends from claim 4, claims vias connecting the juxtaposed parallel wiring lines of the top and bottom portions wherein the vias are spaced along the length of the parallel wiring lines.

Ahn discloses only paths 140 between the top and bottom portions 220 of the inductor. These paths 140 are equivalent to the side portions of Appellants' inductor. However, Ahn can not show vias between the juxtaposed parallel wiring lines of the top and bottom portions of each turn of the inductor and along the length of the parallel wiring lines because Ahn does not show parallel wiring lines of the top and bottom portions of each turn of the inductor and, in addition, does not show vias between those parallel wiring lines and spaced along the length thereof as claimed by Appellants in claim 6.

In the final Office Action, the Examiner states that Ahn illustrates "that the parallel conductive segments (220) have a length and the vias (140) are spaced along the length of the segments (220)." Besides the fact that Ahn does not show top and bottom portions which each comprise parallel wiring lines, and therefore Ahn cannot show vias between those parallel wiring lines, Ahn also does not show vias spaced along the length of the segments (220) as claimed by Appellants. The vias in Ahn are only at the ends of the segments (220) as clearly shown in Figure 1A of Ahn. As Ahn fails to show this limitation of claim 6, Ahn cannot anticipate Appellants' claim 6.

II. The §103 rejections:

A. Claim 7 has been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Ahn in view of Burghartz et al. U.S. Patent 5,884,990.

Inasmuch as claim 7 depends from claim 1 and since claim 1 is believed to be patentable, then claim 7 should be patentable as well. No independent ground of patentability is asserted for claim 7 at this time.

B. Claims 8 to 10 and 13 have been rejected by the Examiner under 35 USC §103(a) as being

unpatentable over Ahn in view of Liu et al. U.S. Patent 6,459,352 (hereafter "Liu").

Inasmuch as claims 8 to 10 and 13 depend from claim 1, and since claim 1 is believed to be patentable, then claims 8 to 10 and 13 are believed to be patentable as well. In addition, claims 9 and 10 are believed to be independently patentable.

"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." MPEP §2143.03. "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 ((CCPA 1970).

As Appellants will argue, each of claims 9 and 10 contain limitations which are not taught or suggested by the prior art, thereby compelling the conclusion that claims 9 and 10 are not rendered obvious by the prior art.

(i) Patentability of claim 9

As Appellants noted above, Ahn does not teach the basic aspects of Appellants' invention. Claim 9 recites an additional feature of Appellants' invention, namely tuning the inductor by deleting a

portion of the inductor.

It is submitted that the Examiner has failed to state a prima facie case of obviousness.

Neither Ahn nor Liu teaches the aspects of Appellants' invention claimed in claim 9. Ahn teaches a single inductor while Liu teaches a transformer, which essentially is an inductor coiled within another inductor. Neither of Ahn nor Liu teaches tuning of the inductor. Tuning is performing some operation on the inductor so as to fine tune the amount of inductance obtained (specification, page 15, lines 18-21). Liu does state, as noted by the Examiner, that the size of the inductor is an important factor with respect to the use of the inductor and its Q factor. The solution to this requirement is to make a small size, high Q inductor as taught by Liu. Liu says nothing about tuning an inductor, once the inductor has already been formed, by deleting a portion of the inductor as Appellants have claimed. It is thus submitted that the Examiner has failed to state a prima facie case of obviousness with respect to claim 9 since the combination of Ahn and Liu fail to teach the limitations of claim 9.

(ii) Patentability of claim 10

As Appellants noted above, Ahn does not teach the basic aspects of Appellants' invention. Claim 10 recites additional features of Appellants' invention, namely tuning the inductor by adding at least one additional buried loop to the inductor.

It is submitted that the Examiner has failed to state a prima facie case of obviousness with respect to claim 10.

Neither Ahn nor Liu teaches the aspects of Appellants' invention claimed in claim 10. Ahn teaches a single inductor while Liu teaches a transformer, which essentially is an inductor coiled within another inductor. Neither of Ahn nor Liu teaches tuning of the inductor. Tuning is performing some operation on the inductor so as to fine tune the amount of inductance obtained (specification, page 15, lines 18-21). It is recognized, as noted by the Examiner, that Liu teaches two inductors to form a transformer. However, these inductors at all times appear to be separated from each other and there appears to be no teachings in Liu to connect these two inductors or a portion of each of the inductors to tune the resulting inductor. Liu says nothing about tuning the inductor, once the inductor has already been formed, by adding an additional loop as Appellants have claimed. It is thus submitted that the Examiner has failed to state a prima facie case of obviousness with respect to claim 10 since the combination of Ahn and Liu fail to teach the limitations of claim 10.

C. Claims 11 and 12 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Ahn in view of Eberhardt U.S. Patent 5,461,353 (hereafter "Eberhardt").

Inasmuch as claims 11 and 12 depend from claim 1, and since claim 1 is believed to be patentable, then claims 11 and 12 should be patentable as well. In addition, claims 11 and 12 are believed to be

independently patentable.

As Appellants will argue, each of claims 11 and 12 contain limitations which are not taught or suggested by the prior art, thereby compelling the conclusion that claims 11 and 12 are not rendered obvious by the prior art.

(i) Patentability of claims 11 and 12

It is submitted that the Examiner has failed to state a prima facie case of obviousness with respect to claims 11 and 12.

As Appellants noted above, Ahn does not teach the basic aspects of Appellants' invention. Claims 11 and 12 recite additional features of Appellants' invention, namely tuning the inductor by the addition of a plate adjacent to the inductor. In claim 11, the plate is electrically isolated from the inductor while in claim 12, the plate is electrically connected to the inductor.

Neither Ahn nor Eberhardt teaches the aspects of Appellants' invention claimed in claims 11 and 12. Ahn does not teach tuning of the inductor. While Eberhardt does teach tuning of the inductor, the tuning is done in a different manner than that claimed by Appellants. That is, Eberhardt's inductor is tuned by metallized runners. By cutting a runner, the number of turns of the inductor is increased. As noted by the Examiner in the final Office Action, "In order to increase the inductance value of the

inductor, one or more of the adjustment runners are cut using well known laser trimming equipment or by simply mechanically cutting one or both runners." It is apparent from Eberhardt that only whole turns are added at a time; this is a very coarse adjustment.

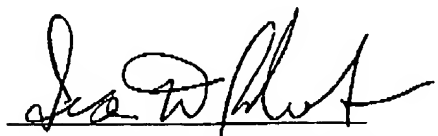
Appellants' invention, on the other hand, uses an adjacent plate to tune the inductor which is structurally different than the metallized runners of Eberhardt. The plate is always there and always affects the inductance of the inductor because the adjacent plate is always magnetically or electrically coupled to the inductor. Any fine tuning can be done by deleting portions of the plate. Thus, Appellants' tuning apparatus as claimed in claims 11 and 12 is structurally different than the metallized runners in Eberhardt and operates functionally differently as well as just explained. Accordingly, the Examiner has failed to state a prima facie case of obviousness since the combination of Ahn and Eberhardt fails to teach the limitations of Appellants' claims 11 and 12.

SUMMARY:

In view of all of the preceding remarks, it is submitted that claims 1, 2, 4 to 13 and 21 to 23 are in condition for allowance, that the Examiner's various rejections of claims 1, 2, 4 to 13 and 21 to 23 are erroneous and reversal of the Examiner's decisions is respectfully requested.

Respectfully Submitted,

David C. Long, et al.



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CLAIMS APPENDIX:

1. A dielectric substrate having a multiturn inductor comprising:

a) a multilayer dielectric body comprising a plurality of layers;

b) a multiturn inductor buried within the dielectric body, each turn of the inductor comprising a bottom portion, a top portion and two side portions, the bottom portion and top portion being parallel and in different layers of the dielectric body, the side portions being parallel to each other and extending between the top and bottom portions and comprising vias in the dielectric body, wherein the top and bottom portions have a lower crossectional area than the side portions and wherein the top and bottom portions each comprise two parallel wiring lines in juxtaposition.

2. The dielectric substrate of claim 1 wherein the top and bottom portions comprise wiring lines situated in respective layers of the dielectric body.

Claim 3. (Canceled)

4. The dielectric substrate of claim 1 further comprising vias connecting the parallel wiring lines of each of the top and bottom portions.

5. The dielectric substrate of claim 4 wherein the parallel wiring lines have ends and wherein the vias connecting the parallel wiring lines are only at the ends of the lines.

6. The dielectric substrate of claim 4 wherein the parallel wiring lines each have a length and wherein the vias connecting the parallel wiring lines are spaced along the length of the parallel wiring lines.

7. The dielectric substrate of claim 1 wherein the turns of the multiturn inductor form a toroidal shape.

8. The dielectric substrate of claim 1 wherein the multiturn inductor is tuned by tapping the multiturn inductor at selected locations.

9. The dielectric substrate of claim 8 further comprising deletion of a portion of the multiturn inductor so as to tune the multiturn inductor.

10. The dielectric substrate of claim 1 wherein the multiturn inductor is tuned by the addition of at least one additional buried loop to the multiturn inductor.

11. The dielectric substrate of claim 1 wherein the multiturn inductor is tuned by the addition of a plate adjacent to the multiturn inductor, the plate being electrically isolated from the multiturn inductor.

12. The dielectric substrate of claim 1 wherein the multiturn inductor is tuned by the addition of a plate adjacent to the multiturn inductor, the plate being electrically connected to the multiturn inductor.

13. The dielectric substrate of claim 1 wherein the multiturn inductor is a first multiturn inductor and further comprising a second buried multiturn inductor near the first multiturn inductor but electrically isolated therefrom, the first and second multiturn inductors cooperating to form a transformer.

Claims 14 to 20 (Canceled).

21. The dielectric substrate of claim 1 wherein the top and bottom portions are planar in shape so as to comprise a flat portion having a width and a thickness less than the width, the side portions having a circular contact surface and the flat portion of the top and bottom portions in contact with the circular contact surface of the side portion.

22. The dielectric substrate of claim 1 wherein the top and bottom portions are planar wiring lines and the side portions are vias having a circular contact surface wherein the planar wiring lines directly contact the circular contact surface of the vias.

23. A dielectric substrate having a multiturn inductor comprising:

a) a multilayer dielectric body comprising a plurality of layers;

b) a multiturn inductor buried within the dielectric body, each turn of the inductor comprising a bottom portion, a top portion and two side portions, the bottom portion and top portion being parallel and in different layers of the dielectric body, the side portions being parallel to each other and extending between the top and bottom portions and comprising vias in the dielectric body, wherein the top and bottom portions have a lower crossectional area than the side portions and wherein the top and bottom portions each comprise at least two parallel wiring lines of unequal length in juxtaposition.

EVIDENCE APPENDIX:

COPIES OF REFERENCES CITED BY THE EXAMINER TO FOLLOW

Ahn et al. U.S. Patent 6,531,945

Burghartz et al. U.S. Patent 5,884,990

Eberhardt U.S. Patent 5,461,353

Liu et al. U.S. Patent 6,459,352

RELATED PROCEEDINGS APPENDIX

NO RELATED PROCEEDINGS

US006531945B1

(12) **United States Patent**
Ahn et al.

(10) **Patent No.: US 6,531,945 B1**
(45) **Date of Patent: Mar. 11, 2003**

(54) **INTEGRATED CIRCUIT INDUCTOR WITH A MAGNETIC CORE**

(75) Inventors: **Kie Y. Ahn**, Chappaqua, NY (US); **Leonard Forbes**, Corvallis, OR (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/523,097

(22) Filed: Mar. 10, 2000

(51) Int. Cl.[7] H01F 5/00

(52) U.S. Cl. 336/200; 336/223; 336/232; 29/602.1

(58) Field of Search 336/200, 223, 336/232; 29/206, 202.1

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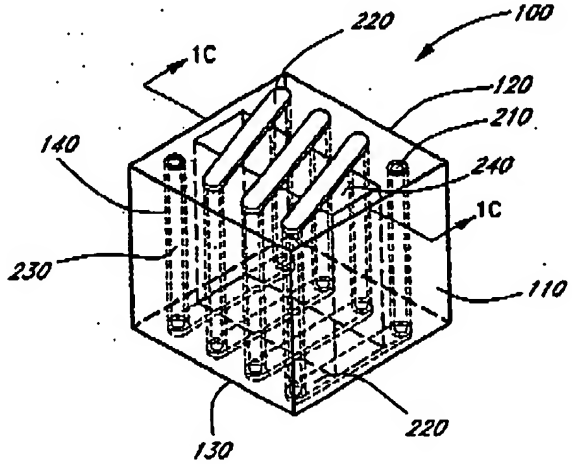
(74) *Attorney, Agent, or Firm*—Knobbe, Martens, Olson & Bear, LLP

(57) ABSTRACT

An inductor is fabricated on a substrate having a top surface and a bottom surface. The inductor includes a plurality of holes extending through the substrate, wherein the plurality of holes interconnect the top surface and the bottom surface of the substrate. The inductor also includes a plurality of conductive posts formed in the plurality of holes and a plurality of conductive segments formed on the top surface and on the bottom surface that interconnect the conductive posts such that a continuous conductive coil is formed. The inductor also includes a magnetic core that occupies substantially the entire volume enclosed by the conductive coil.

15 Claims, 10 Drawing Sheets



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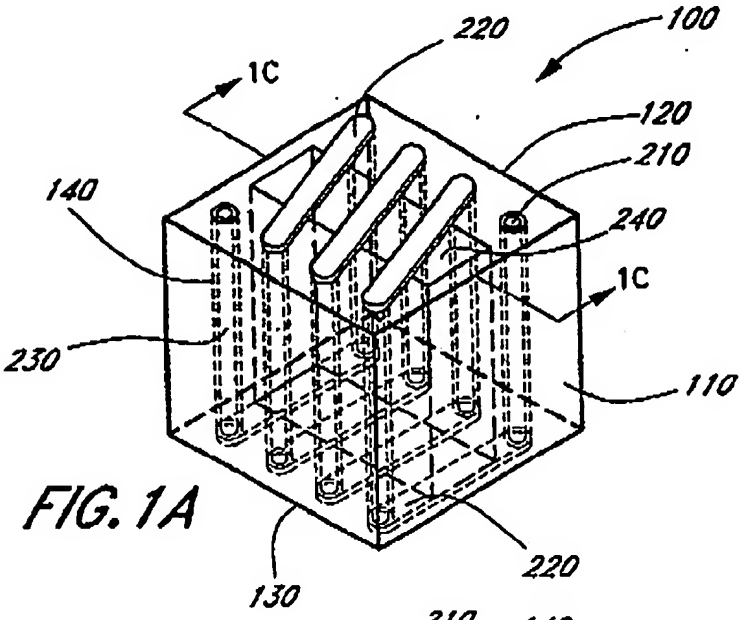

FIG. 1A

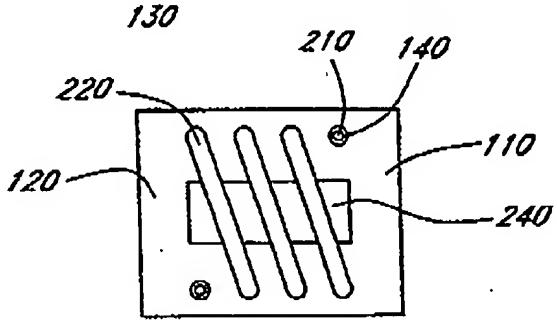

FIG. 1B

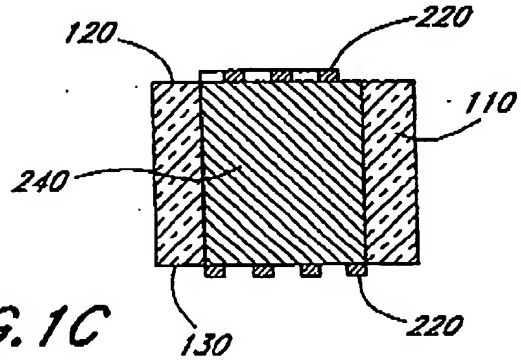

FIG. 1C

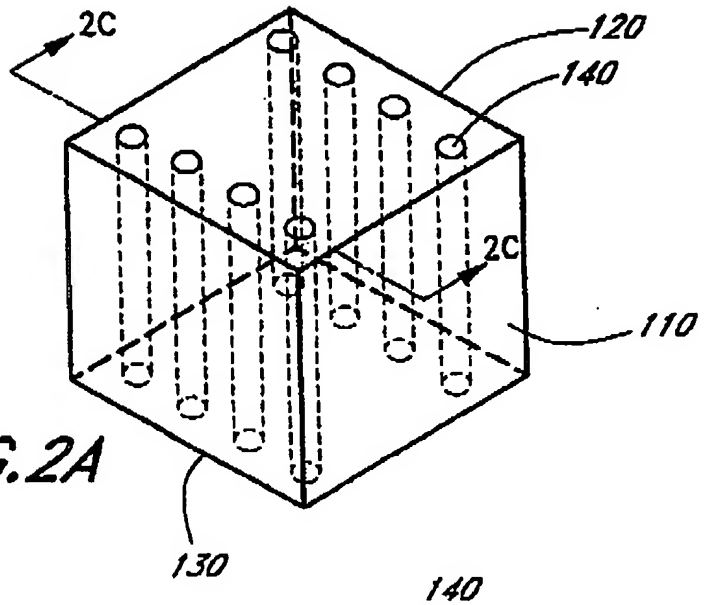

FIG. 2A

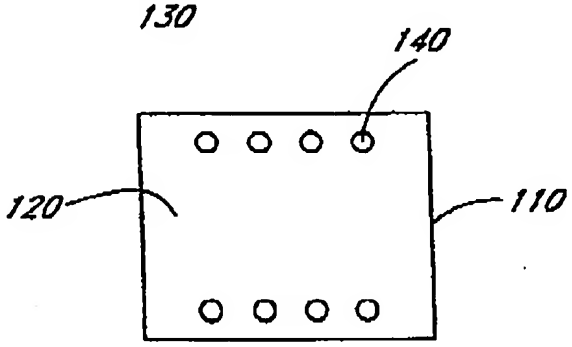

FIG. 2B

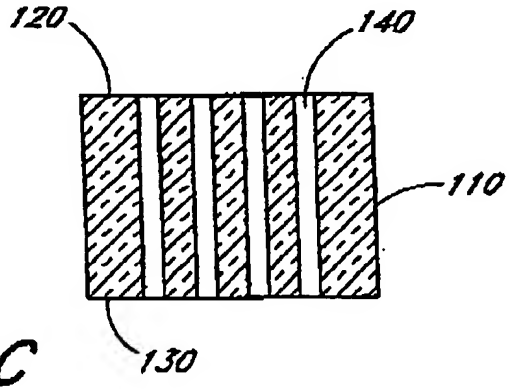

FIG. 2C

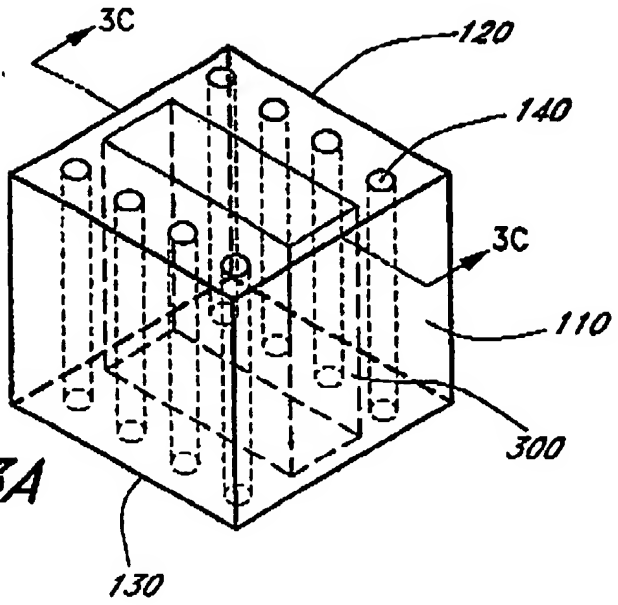

FIG. 3A

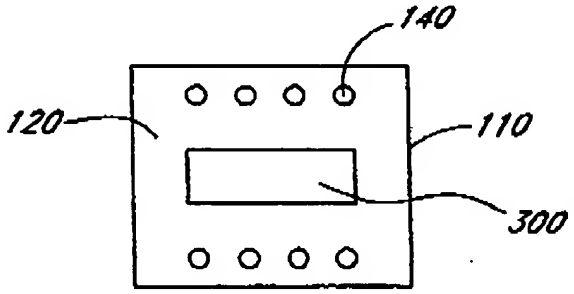

FIG. 3B

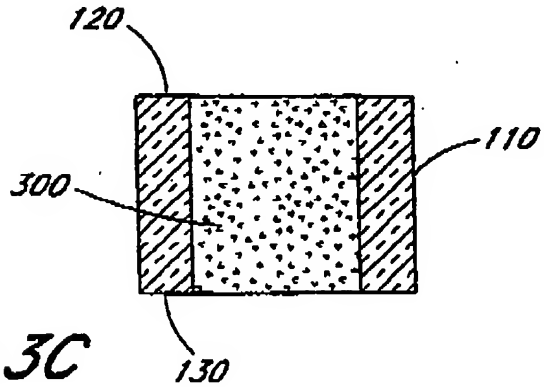

FIG. 3C

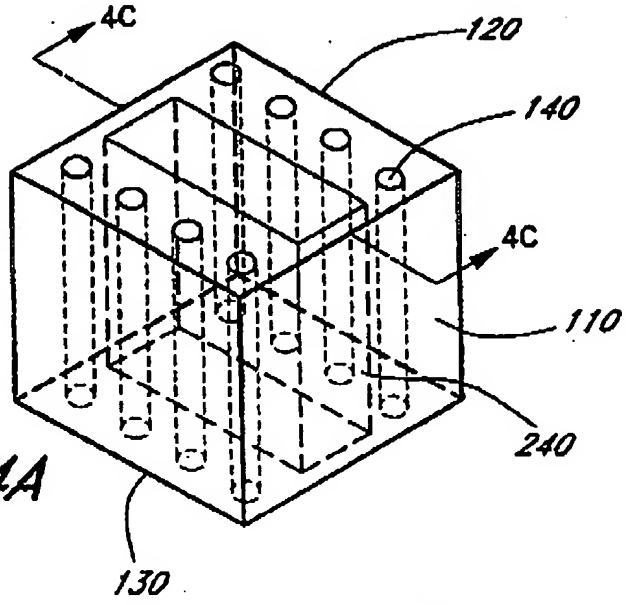

FIG. 4A

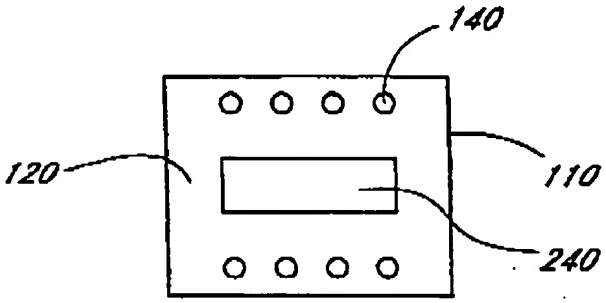

FIG. 4B

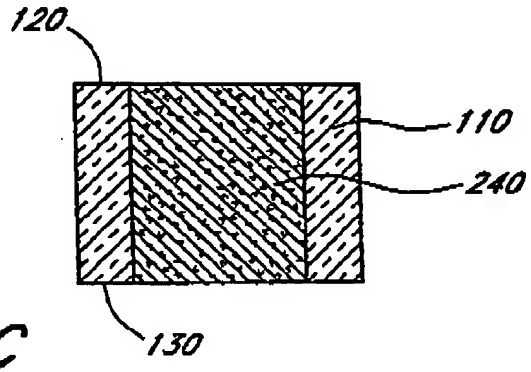

FIG. 4C

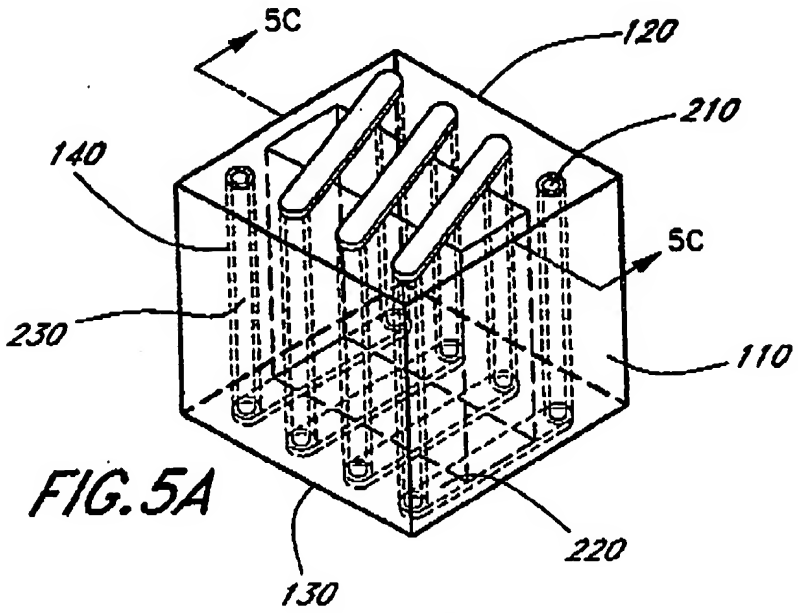

FIG. 5A

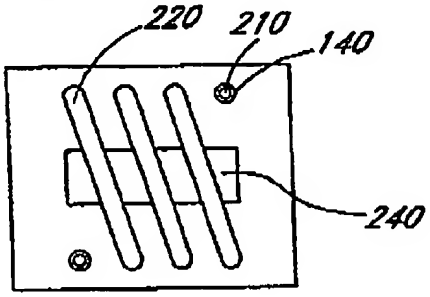

FIG. 5B

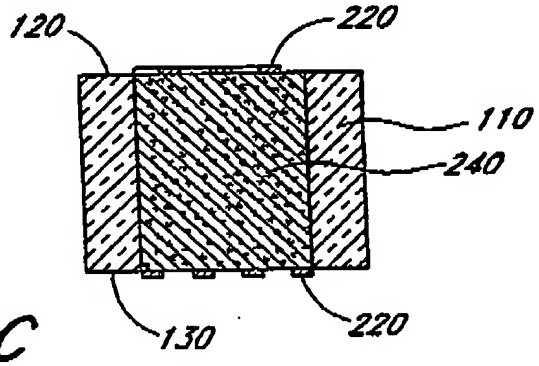

FIG. 5C

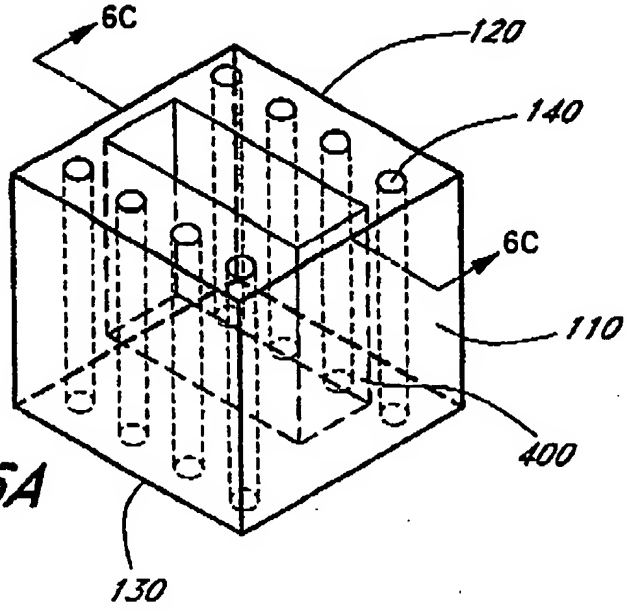

FIG. 6A

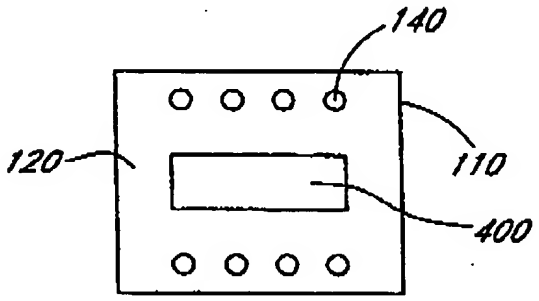

FIG. 6B

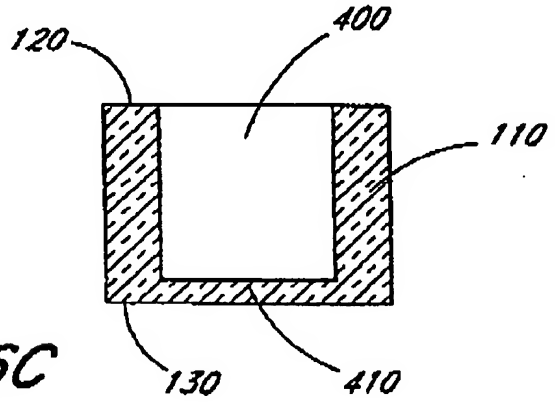

FIG. 6C

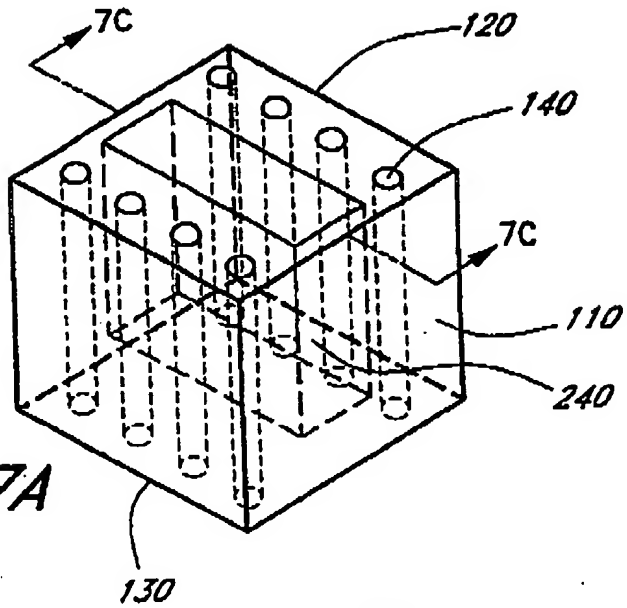

FIG. 7A

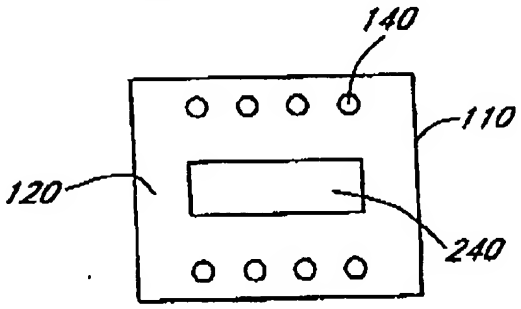

FIG. 7B

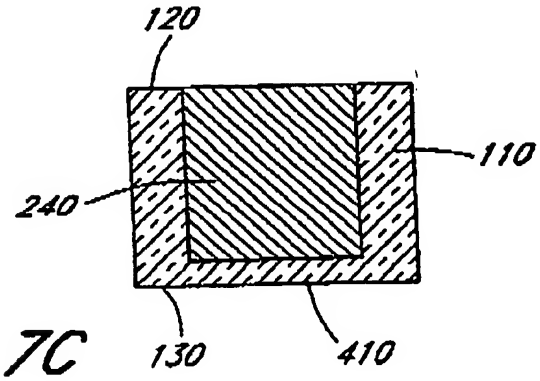

FIG. 7C

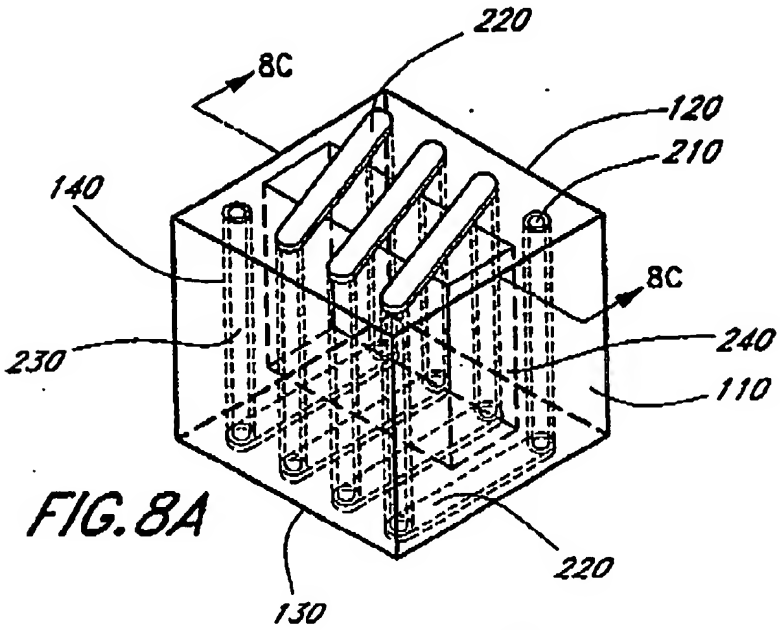

FIG. 8A

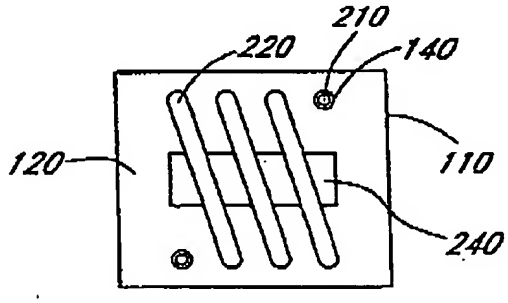

FIG. 8B

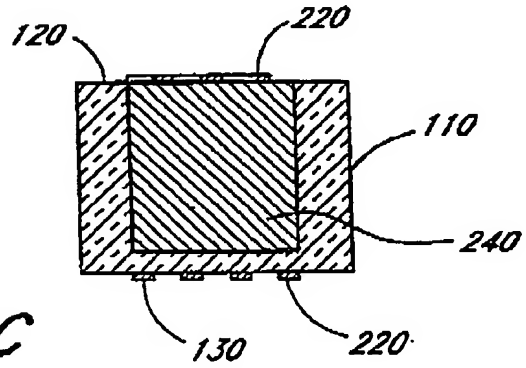

FIG. 8C

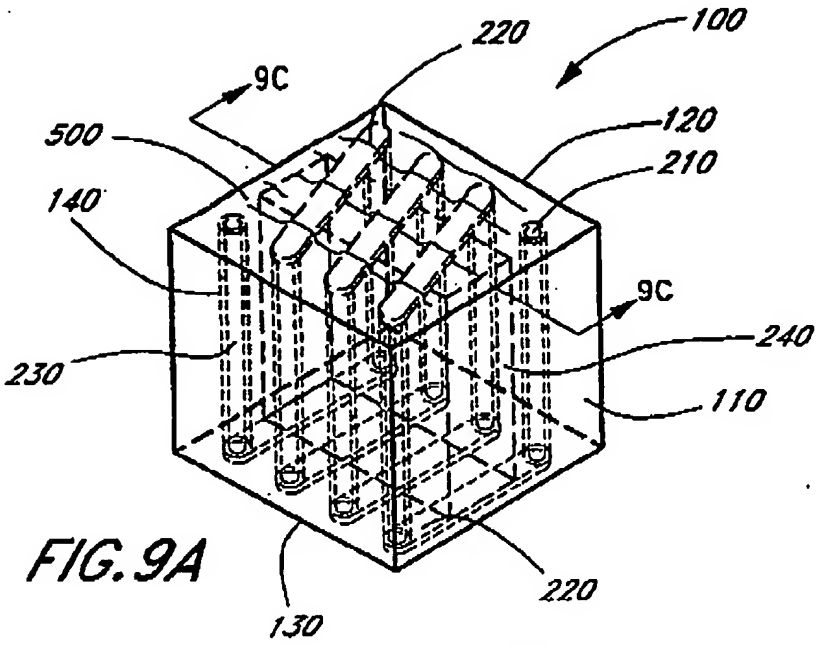

FIG. 9A

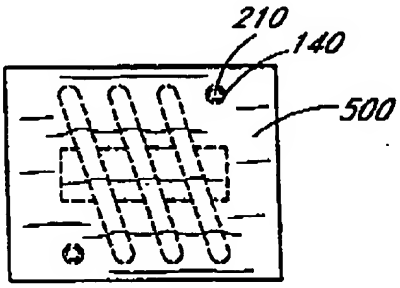

FIG. 9B

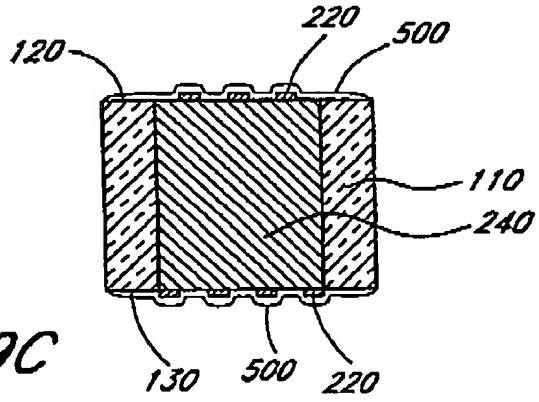

FIG. 9C

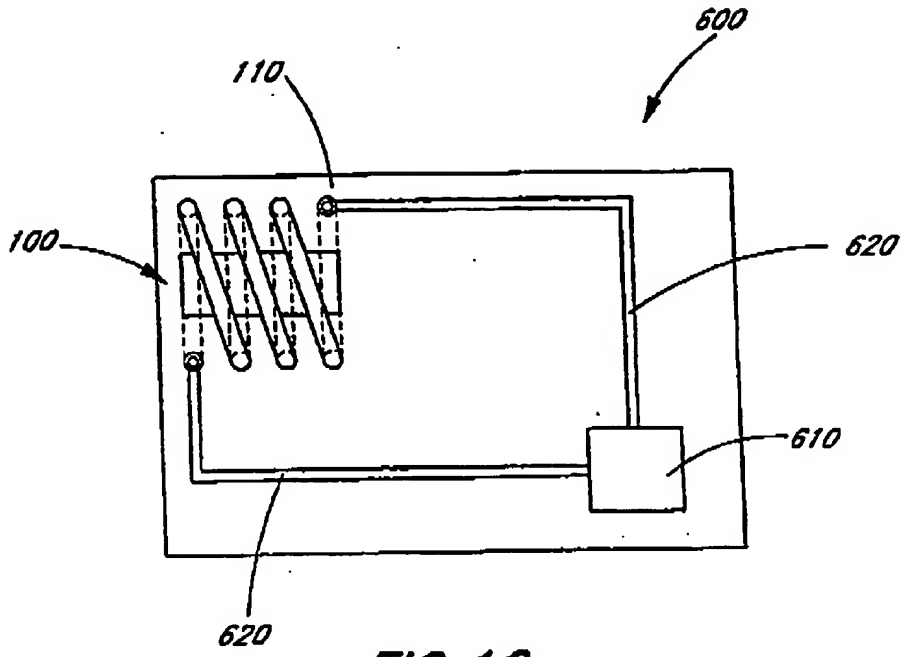
600
110
100
620
610
620

FIG. 10

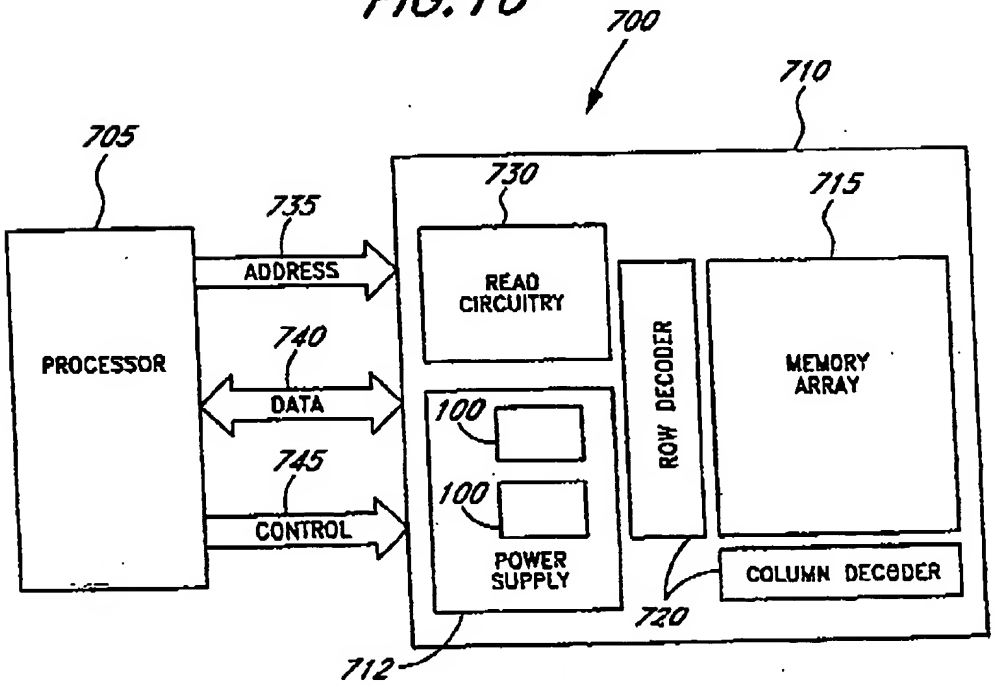
700
710
705
730
715
735
ADDRESS
READ CIRCUITRY
ROW DECODER
MEMORY ARRAY
PROCESSOR
740
DATA
100
745
100
CONTROL
POWER SUPPLY
COLUMN DECODER
720
712

FIG. 11

INTEGRATED CIRCUIT INDUCTOR WITH A MAGNETIC CORE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates in general to inductors for use in integrated circuits, and relates more particularly to integrated circuit inductors having magnetic cores.

2. Description of the Related Art

Inductors are used in a wide range of signal processing systems and circuits. For example, inductors are used in communication systems, radar systems, television systems, high pass filters, tank circuits, and butterworth filters.

As electronic signal processing systems have become more highly integrated and miniaturized, system designers have sought to eliminate the use of relatively large auxiliary components, such as inductors. One approach to eliminating the use of actual inductors in signal processing systems is to simulate inductors using active circuits, which can be easily miniaturized. Unfortunately, simulated inductor circuits tend to exhibit large parasitic effects and often generate more noise than circuits constructed using actual inductors.

When unable to eliminate inductors in their designs, designers have sought ways to reduce the size of the inductors that are used. For example, inductors are miniaturized for use in compact communication systems, such as cellular phones and modems. These miniaturized inductors typically comprise two-dimensional spiral inductors that are fabricated on the same substrates as the integrated circuits to which they are coupled. Although these two-dimensional spiral inductors can be fabricated using conventional integrated circuit manufacturing techniques, they typically take up a disproportionately large share of the available surface area on an integrated circuit substrate.

For these and other reasons, there is a need for the present invention.

SUMMARY OF THE INVENTION

An inductor comprises a substrate, a magnetic core formed in a region of the substrate, and a conductive coil interwoven with the substrate and surrounding the magnetic core.

In one embodiment, an inductor comprises a substrate, a magnetic core formed on the substrate, and a three-dimensional conductive coil. The conductive coil comprises a plurality of conductive posts interconnected by a plurality of conductive segments such that the conductive coil surrounds the magnetic core.

In one embodiment, an inductor comprises a substrate comprising a semiconductor having a crystalline structure, a magnetic core formed on the substrate, a plurality of paths extending through the substrate, and a conductive coil woven through the plurality of paths and surrounding the magnetic core. The conductive coil is at least partially diffused into the crystalline structure.

In one embodiment, a device comprises a substrate and an inductive structure having an inductance of at least 1 nanohenry (nH). The inductive structure includes a magnetic core and is at least partially embedded in the substrate.

In one embodiment, an inductor comprises a substrate, a magnetic core formed on the substrate, a pair of substantially parallel rows of conductive posts providing a plurality of conductive paths through the substrate, and a plurality of conductive segments interconnecting the pair of substantially parallel rows of conductive columns to form a conductive coil surrounding the magnetic core.

In one embodiment, an inductor comprises a perforated substrate, a magnetic core formed on the perforated substrate, and a conductive material interwoven with the perforated substrate and surrounding the magnetic core. The conductive material is at least partially diffused into the perforated substrate.

In one embodiment, an inductor comprises a substrate having a top surface and a bottom surface, a plurality of holes extending through the substrate, wherein the plurality of holes interconnect the top surface and the bottom surface. The inductor further comprises a plurality of conductive posts formed in the plurality of holes, a plurality of conductive segments formed on the top surface and on the bottom surface that interconnect the conductive posts such that a continuous conductive coil is formed; and a magnetic core occupying substantially the entire volume enclosed by the conductive coil.

In one embodiment, an inductor comprises a multilayer substrate, a magnetic core formed on the multilayer substrate, and a coil interwoven with the multilayer substrate and surrounding the magnetic core.

In one embodiment, a device comprises an integrated circuit formed on a substrate, a magnetic core formed on the substrate, and an inductor interwoven with the substrate and surrounding the magnetic core, wherein the inductor is operably coupled to the integrated circuit.

In one embodiment, a memory system comprises a substrate having a plurality of memory circuits, a magnetic core formed in a region of the substrate, and a conductive coil interwoven with the substrate and surrounding the magnetic core.

In one embodiment, a computer system comprises a processor and an inductor comprising a substrate, a magnetic core formed on the substrate, and a conductive coil interwoven with the substrate and surrounding the magnetic core. The computer system further comprises an electronic device coupled to the inductor and to the processor.

In one embodiment, a method of fabricating an inductor embedded in a substrate comprises the steps of forming a magnetic core in the substrate and fabricating a three-dimensional conductive coil around the magnetic core.

In one embodiment, a method of fabricating an inductor embedded in a substrate comprises the steps of forming a plurality of paths extending through the substrate, forming a magnetic core in the substrate, depositing a conductive material in the paths to form a plurality of conductive posts, and fabricating a plurality of conductive segments that interconnect the conductive posts to form a conductive coil.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A–1C illustrate an embodiment of an inductor in accordance with the present invention.

FIGS. 2A–2C illustrate a substrate with a plurality of paths extending through the substrate.

FIGS. 3A–3C illustrate the substrate of FIGS. 2A–2C after a region of the substrate has been treated to form a porous region.

FIGS. 4A–4C illustrate the substrate of FIGS. 3A–3C after the porous region has been treated with a ferromagnetic material to form a magnetic core.

FIGS. 5A–5C illustrate the substrate of FIGS. 4A–4C after the paths have been filled with a conductive material and interconnected to form a conductive coil.

FIGS. 6A–6C illustrate the substrate of FIGS. 2A–2C after a cavity has been formed in a region of the substrate.

FIGS. 7A–7C illustrate the substrate of FIGS. 6A–6C after the cavity has been filled with a ferromagnetic material to form a magnetic core.

FIGS. 8A–8C illustrate the substrate of FIGS. 7A–7C after the paths have been filled with a conductive material and interconnected to form a conductive coil.

FIGS. 9A–9C illustrate an embodiment of an inductor in accordance with the present invention after the formation of two passivation layers around the inductor.

FIG. 10 illustrates a top view of an embodiment of an inductor-coupled circuit in accordance with the present invention.

FIG. 11 illustrates a block diagram of a system level embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1A illustrates an isometric view of an embodiment of an inductor **100** in accordance with the present invention. FIG. 1B illustrates a top view of the inductor **100** shown in FIG. 1A. FIG. 1C illustrates a cross-sectional view of the inductor **100** along the line 1C—1C shown in FIG. 1A. In the illustrated embodiment, the inductor **100** is fabricated on a substrate **110**. In one embodiment, the substrate **110** is fabricated from a crystalline material. In an alternative embodiment, the substrate **110** is fabricated from a single-element doped or undoped semiconductor material, such as silicon or germanium. In further embodiments, the substrate **110** is fabricated from gallium arsenide, from silicon carbide, or from a partially magnetic material having a crystalline or amorphous structure.

Those of ordinary skill in the art will understand that the substrate **110** is not limited to a single layer substrate. Multiple layer substrates, coated or partially coated substrates, and substrates having a plurality of coated surfaces are all suitable for use in connection with the present invention. Suitable coatings may include insulators, ferromagnetic materials, and magnetic oxides. Insulators protect the inductive coil and separate the electrically conductive inductive coil from other conductors, such as signal carrying circuit lines. Coatings and films of ferromagnetic materials, such as magnetic metals, alloys, and oxides, increase the inductance of the inductor **100**.

In addition, those of ordinary skill in the art will understand that the substrate **110** may be the fabrication site for a wide variety of integrated circuits and circuit components in addition to the inductor **100**. In one embodiment, for example, the substrate **110** is the fabrication site for the inductor **100** and for a Dynamic Random Access Memory (DRAM) circuit.

In another embodiment, the substrate **110** comprises a package, such as a ceramic package, for an electronic device. This embodiment allows circuits to be designed with off-chip inductors in accordance with the present invention. By fabricating off-chip inductors in accordance with the present invention, the fabrication cost of the inductors is advantageously reduced.

In FIGS. 1A–1C, the substrate **110** has a top surface **120** and a bottom surface **130**. Those of ordinary skill in the art will understand that the top surface **120** and the bottom surface **130** are not limited to oblique surfaces. In one embodiment, the top surface **120** and the bottom surface **130** are substantially parallel to one another. Because many integrated circuit manufacturing processes are designed to work with substrates having a pair of relatively flat parallel surfaces, the use of parallel surfaces may simplify the manufacturing process for forming the inductor **100**.

The substrate **110** has a plurality of paths **140** extending through the substrate **110**. The paths **140** interconnect the top surface **120** and the bottom surface **130** of the substrate **110**. The paths **140** can advantageously comprise holes, vias, perforations, or any other suitable paths that can be filled, plugged, partially filled, partially plugged, or lined with a conducting material. In one embodiment, the plurality of paths **140** are substantially parallel to each other and are substantially perpendicular to the top surface **120** and to the bottom surface **130** of the substrate **110**.

In FIGS. 1A–1C, the paths **140** are filled by a plurality of conductive posts **210**. The conductive posts **210** are conductively interconnected by a plurality of conductive segments **220** located on the top surface **120** and on the bottom surface **130** of the substrate **110**. The conductive posts **210** and the conductive segments **220** are interconnected to form a three-dimensional conductive coil **230**, which is interwoven with the substrate **110**. Thus, the inductor **100** is at least partially embedded in the substrate **110**. Those of ordinary skill in the art will understand that the cross-sectional profile of the conductive posts **210** or of the conductive segments **220** is not limited to any particular shape. For example, rectangular, square, circular, and triangular shapes are all suitable for use in connection with the present invention.

In the illustrated embodiment, the conductive posts **210** are configured in two substantially parallel rows. The rows are interconnected by the plurality of conductive segments **220** to form a plurality of loops. Those of ordinary skill in the art will understand that the shape of each loop in the conductive coil **230** is not limited to any particular geometric shape. For example, rectangular, square, and triangular loops are all suitable for use in connection with the present invention.

The conductive coil **230** surrounds a magnetic core **240** and is capable of producing a reinforcing magnetic field or flux in the volume occupied by the magnetic core **240**. In a preferred embodiment, the magnetic core **240** occupies substantially the entire volume enclosed by the conductive coil **230**. By forming the magnetic core **240** in substantially the entire volume enclosed by the conductive coil **230**, the inductance value of the inductor **100** is advantageously increased. In one embodiment, for example, the inductor **100** preferably has an inductance value in the range of about 10 nanohenries (nH) to about 100 microhenries (μH), more preferably in the range of about 10 nH to about 100 nH.

FIGS. 2–9 illustrate the step-by-step formation of the inductor **100** shown in FIGS. 1A–1C using two alternative methods. FIG. 2A illustrates an isometric view of one embodiment of the substrate **110** with a plurality of paths **140** extending through the substrate **110**. FIG. 2B illustrates a top view of the substrate **110** shown in FIG. 2A. FIG. 2C illustrates a cross-sectional view of the inductor **100** along the line 2C—2C shown in FIG. 2A. The paths **140** interconnect the top surface **120** and the bottom surface **130** of the substrate **110**. The distance between the top surface **120** and the bottom surface **130** of the substrate **110** is typically in the range of about 700 micrometers (μm) to about 800 μm. Therefore, the paths **140** typically have a length in the range of about 700 μm to about 800 μm.

Those of ordinary skill in the art will understand that the paths **140** can be formed using a variety of suitable processes. For example, in a preferred embodiment, the paths

140 are formed using any of a number of well-known etching processes. In other embodiments, a laser or a diamond-tipped carbide drill is used to create the paths 140.

Furthermore, those of ordinary skill in the art will understand that the shape of the paths 140 is not limited to any particular shape. For example, circular, square, rectangular, and triangular shapes are all suitable for use in connection with the present invention.

In one embodiment, the inside of the paths 140 is lined or partially lined with an electrically insulating layer (not shown). The insulating layer may comprise a variety of suitable nonconductive materials, such as, for example, polyimide, a dielectric, or an inorganic oxide, such as silicon dioxide or silicon nitride. The purpose of the insulating layer is to electrically isolate the conductive posts 210 from the magnetic core 240 when these components are formed.

FIGS. 3–5 illustrate the step-by-step formation of the inductor 100 shown in FIGS. 1A–1C using a first exemplary process. Specifically, FIG. 3A illustrates an isometric view of the substrate 110 shown in FIGS. 2A–2C after a region of the substrate 110 has been treated to form a porous region 300. FIG. 3B illustrates a top view of the substrate 110 shown in FIG. 3A. FIG. 3C illustrates a cross-sectional view of the substrate 110 along the line 3C—3C shown in FIG. 3A. The location of the porous region 300 is selected such that the porous region 300 occupies the volume that will be enclosed by the conductive coil 230 when it is fully formed, as described in more detail below. A designer can designate the area on the substrate 110 in which the porous region 300 will be formed using conventional photolithography and masking processes.

Once the area for the porous region 300 has been designated, those of ordinary skill in the art will understand that the porous region 300 can be formed using a variety of suitable processes. For example, in one embodiment, the porous region 300 may be formed using a well-known anodic etching process. In another embodiment, the porous region 300 may be formed using a well-known laser ablation process.

In a preferred embodiment, the porous region 300 penetrates substantially the entire thickness of the substrate 110. This configuration advantageously allows substantially the entire volume enclosed by the conductive coil 230 to form the magnetic core 240 when the inductor 100 is fully fabricated. As discussed above, by forming the magnetic core 240 in substantially the entire volume enclosed by the conductive coil 230, the inductance value of the inductor 100 is advantageously increased.

FIG. 4A illustrates an isometric view of the substrate 110 shown in FIGS. 3A–3C after a ferromagnetic material has been deposited in the porous region 300 to form the magnetic core 240. FIG. 4B illustrates a top view of the substrate 110 shown in FIG. 4A. FIG. 4C illustrates a cross-sectional view of the substrate 110 along the line 4C—4C shown in FIG. 4A. Those of ordinary skill in the art will understand that a variety of ferromagnetic materials can be used to form the magnetic-core 240. For example, in one embodiment, a material comprising Permalloy having about 81% nickel (Ni) and about 19% iron (Fe) is deposited in the porous region 300 of the substrate 110. The magnetic material used to form the magnetic core 240 affects the inductance of the inductor 100 when it is fully fabricated. Thus, the particular magnetic material used to form the magnetic core 240 may advantageously be selected based on the desired inductance value.

In addition, those of ordinary skill in the art will understand that the ferromagnetic material can be deposited in the porous region 300 using a variety of suitable methods. For example, in one embodiment, the ferromagnetic material is deposited in the porous region 300 using a well-known chemical vapor deposition (CVD) process. In other embodiments, the ferromagnetic material is deposited in the porous region 300 using well-known evaporation, sputtering, laser ablation, or electrochemical deposition processes. The particular method used to deposit the ferromagnetic material in the porous region 300 may advantageously be selected based upon available deposition equipment.

In one embodiment, the ferromagnetic material is deposited in the porous region 300 using a CVD process by exposing the porous region 300 to iron pentacarbonyl vapor in an oxidizing atmosphere. In light of the present disclosure, those of ordinary skill in the art can readily determine suitable CVD parameters to achieve the desired ferromagnetic material composition in a given reactor configuration. For example, in one configuration, the iron pentacarbonyl vapor is decomposed at a temperature in the range of about 140° C. to about 200° C., and a deposition rate in the range of about 600 Å/minute to about 1400 Å/minute with an O_2 flow rate of about 60 standard cubic centimeters per minute (sccm) and an Ar flow rate in the range of about 40 sccm to about 60 sccm.

In another embodiment, the ferromagnetic material comprises a gamma iron oxide film, which is deposited in the porous region 300 using a chemical vapor pyrolysis process. If the temperature in the chemical vapor pyrolysis reactor exceeds 500° C., then the gamma oxide film formed in the porous region 300 exhibits magnetic properties. Otherwise, the gamma oxide film formed in the porous region 300 does not exhibit magnetic properties.

In another embodiment, the ferromagnetic material comprises a spinel-type iron oxide film, which can be deposited at low temperature by ECR plasma-enhanced metalorganic chemical vapor deposition (MOCVD). The spinel-type iron oxide film formed in the porous region 300 advantageously exhibits nearly isotropic magnetic properties.

In another embodiment, the ferromagnetic material comprises an amorphous iron oxide film. The film can be formed in the porous region 300 by depositing iron in an oxygen atmosphere by evaporation. A ferrous oxide (FeO) powder is evaporated in a vacuum containing oxygen and having a pressure in the range of about 10^{-5} torr to about 10^{-4} torr.

In another embodiment, the ferromagnetic material is deposited in the porous region 300 using a reactive sputtering process. An iron (Fe) target is sputtered onto the porous region 300 in an atmosphere containing oxygen and a substantially inert gas, such as argon (Ar), at a high deposition rate, such as a rate that is about ten times higher than the typical deposition rate. The sputtering process creates an alpha iron oxide film, which is converted to a magnetic gamma type by reducing the film in an atmosphere containing hydrogen.

In another embodiment, the ferromagnetic material is deposited in the porous region 300 using a direct sputtering process. Hot-pressed cobalt (Co) and titanium-doped ferrous oxide (Fe_2O_4) are used as the target in a sputtering reactor.

In another embodiment, the ferromagnetic material comprises gamma iron oxide films, which are deposited in the porous region 300 using an RF glow discharge process with iron pentacarbonyl vapor. In this embodiment, the gamma iron oxide films are formed by introducing either oxygen or carbon dioxide with iron pentacarbonyl into a glow discharge reactor at temperature above about 200° C. This process creates amorphous iron-containing and crystalline iron oxide films having a particle size less than about 0.1 μm.

In another embodiment, the ferromagnetic material comprises iron oxide and ferrite films, which are deposited in the porous region 300 using a pulsed ruby laser evaporation process. The properties of the films are affected by the substrate temperature and oxygen partial pressure during deposition. Thus, the properties of the films can advantageously be controlled by adjusting the substrate temperature and oxygen partial pressure during deposition.

In another embodiment, the ferromagnetic material comprises iron oxide films, which are deposited in the porous region 300 using the plume generated by the excimer laser ablation of polyferric methacrylate, a metal-containing polymer. The iron oxide films deposited using this process comprise iron-rich Fe_3O_4 and alpha Fe_2O_3.

In another embodiment, the ferromagnetic material comprises Fe_2O_3 and Ba-containing iron oxide films, which are deposited in the porous region 300 by ferrite plating with chelated high-alkaline aqueous solutions. The Fe_2O_3 and Ba-containing iron oxide films are formed from chelated high-alkaline aqueous solutions by ferrite plating on the substrate 110, which is heated by lamp beams. The solubility limit of the Ba-containing iron oxide films is about Ba/Fe=0.16.

FIG. 5A illustrates an isometric view of the substrate 110 shown in FIGS. 4A–4C after the conductive posts 210 and the conductive segments 220 have been fabricated and interconnected to form the conductive coil 230. FIG. 5B illustrates a top view of the substrate 110 shown in FIG. 5A. FIG. 5C illustrates a cross-sectional view of the substrate 110 along the line 5C—5C shown in FIG. 5A. Those of ordinary skill in the art will understand that the conductive posts 210 and the conductive segments 220 can be fabricated from a wide variety of suitable conductive materials, such as metals (e.g., aluminum, copper, gold, and the like), alloys, doped polysilicon, metal suicides, and the like. In general, materials having a higher conductivity are preferred to materials having a lower conductivity.

In one embodiment, the conductive material is used to fill or partially fill the paths 140 to form the plurality of conductive posts 210. In an alternative embodiment, the conductive coil 230 is partially diffused into the substrate 110.

In one embodiment, each conductive post 210 and conductive segment 220 is fabricated from a different conductive material. This configuration is particularly advantageous because the properties of the conductive coil 230 can be easily tuned through the selection of the various conductive materials. For example, the internal resistance of the conductive coil 230 can be increased by selecting a material having a higher resistance for a particular conductive segment 220 than the average resistance in the rest of the conductive coil 230.

In an alternate embodiment, two different conductive materials are selected for fabricating the conductive coil 230. In this embodiment, materials are selected based on their compatibility with the available integrated circuit manufacturing processes. For example, if it is difficult to create a barrier layer where the conductive coil 230 pierces the substrate 110, then the conductive posts 210 that pierce the substrate 110 can be fabricated from aluminum. On the other hand, if it is relatively easy to create a barrier layer for the conductive segments 220 that interconnect the conductive posts 210, then copper can be used for the conductive segments 220.

FIGS. 6–9 illustrate the step-by-step formation of the inductor 100 shown in FIGS. 1A–1C using a second exemplary method. Specifically, FIG. 6A illustrates an isometric view of the substrate 110 shown in FIGS. 2A–2C after a cavity 400 has been formed in a region of the substrate 110. FIG. 6B illustrates a top view of the substrate 110 shown in FIG. 6A. FIG. 6C illustrates a cross-sectional view of the substrate 110 along the line 6C—6C shown in FIG. 6A. The location of the cavity 400 is selected such that the cavity 400 occupies the volume that will be enclosed by the conductive coil 230 when it is fully formed, as described in more detail below. A designer can designate the area on the substrate 110 in which the cavity 400 will be formed using conventional photolithography and masking processes.

Once the area for the cavity 400 has been designated, those of ordinary skill in the art will understand that the cavity 400 can be formed using a variety of suitable processes. For example, the cavity 400 may be formed using any of a number of well-known etching processes.

In a preferred embodiment, the cavity 400 is formed such that a layer 410 of the substrate 110 remains under the cavity 400. Preferably, the layer 410 has a thickness in the range of about 20 μm to about 30 μm. As discussed above, the substrate typically has a thickness in the range of about 700 μm to about 800 μm. Thus, the cavity 400 penetrates substantially the entire thickness of the substrate 110. This configuration advantageously allows substantially the entire volume enclosed by the conductive coil 230 to form the magnetic core 240 when the inductor 100 is fully fabricated. As discussed above, by forming the magnetic core 240 in substantially the entire volume enclosed by the conductive coil 230, the inductance value of the inductor 100 is advantageously increased.

FIG. 7A illustrates an isometric view of the substrate 110 shown in FIGS. 6A–6C after a ferromagnetic material has been deposited in the cavity 400 to form the magnetic core 240. FIG. 7B illustrates a top view of the substrate 110 shown in FIG. 7A. FIG. 7C illustrates a cross-sectional view of the substrate 110 along the line 7C—7C shown in FIG. 7A. Those of ordinary skill in the art will understand that a variety of ferromagnetic materials can be used to form the magnetic core 240. For example, a material comprising a polymer magnet or magnetic particles mixed in a polymer can be deposited in the cavity 400. The magnetic material used to form the magnetic core 240 affects the inductance of the inductor 100 when it is fully fabricated. Thus, the particular magnetic material used to form the magnetic core 240 may advantageously be selected based on the desired inductance value.

In addition, those of ordinary skill in the art will understand that the ferromagnetic material can be deposited in the cavity 400 using a variety of suitable processes. For example, the ferromagnetic material can be cast or spin coated to fill the cavity 400. Alternatively, the ferromagnetic material can be deposited in the cavity 400 using well-known chemical vapor deposition (CVD), evaporation, sputtering, laser ablation, or electrochemical deposition processes. The particular process used to deposit the ferromagnetic material in the cavity 400 may advantageously be selected based upon available deposition equipment.

In one embodiment, the ferromagnetic material comprises micromachinable magnetic polymer composites, which are deposited in the cavity 400 using commercial polyimide (Dupont PI-2555) and ferrite magnetic powders.

In another embodiment, the ferromagnetic material comprises polymer-bound iron particle core, which is deposited in the cavity 400 by mixing spherical iron particles having a size in the range of about 6 μm to about 10 μm with 2%

(by weight) of soluble imide. The mixture is compression molded at a temperature of about 300° C. and at a pressure of about 131 megaPascals (MPa). The mixture can be annealed at a temperature of about 960° C. for a time period of about 6 hours to advantageously enhance the permeability in low field region.

In another embodiment, the ferromagnetic material comprises monolayer and multilayer ultrathin films composed of nanosized iron oxide (Fe_3O_4) particles and polyimide molecules, which are deposited in the cavity 400 using a layer-by-layer electrostatic self-assembly process. The substrate is first dipped into an aqueous solution of an anionic polyimide precursor (polyamic acid salt, PAATEA), and then dipped into an aqueous of polycation polydiallydimethylammonium chloride (PDDA) which coats on the nanoscale Fe_3O_4 as a stabilizer.

In another embodiment, the ferromagnetic material comprises a composite of Fe—Co with a copolymer of aniline formaldehyde, which is deposited in the cavity 400 using chemical processing.

In another embodiment, the ferromagnetic material comprises thin films consisting of granular dispersions of cobalt nano-particles in a hydrocarbon matrix, which are deposited in the cavity 400 by the sputtering of cobalt and the polymerization of hydrocarbon. The process involves the simultaneous sputtering of cobalt and plasma-induced polymerization of hydrocarbon monomers. The cobalt nanoparticles advantageously exhibit a hexagonal close-packed (hcp) structure and are uniformly distributed throughout the amorphous hydrocarbon matrix.

In another embodiment, the ferromagnetic material comprises a polymer magnetic composite (PMC) composed of ferrite powder, polymer, and solvent.

In another embodiment, the ferromagnetic material comprises a composite material consisting of a thermoplastic elastomer incorporated with iron powder and nickel-iron alloy powder.

In another embodiment, the ferromagnetic material comprises a composite of polyaniline (PANI), which is deposited in the cavity 400 using a chemical method. The saturation magnetization of the material advantageously increases as the reaction temperature and the concentration of $FeSO_4$ solution increases.

In another embodiment, the ferromagnetic material comprises ferromagnetic particle composite (FPC) films, which are deposited in the cavity 400 using a conventional spin-coating method. The FPC films are composed of polymers in which very fine ferromagnetic particles are homogeneously dispersed.

By depositing the ferromagnetic material in the cavity 400 using one of the processes discussed above or using any other suitable process, the magnetic core 240 is formed. Because the formation of the magnetic core 240 using this method involves low temperature materials, this method is particularly advantageous for low-temperature packaging of laminated printed circuit boards and silicon interposers. Those of ordinary skill in the art will understand that interposers are used for mounting semiconductor devices on circuit boards. After the magnetic core 240 is formed, the top surface 120 of the substrate 110 is preferably micromachined to provide a smooth surface.

FIG. 8A illustrates an isometric view of the substrate 110 shown in FIGS. 7A–7C after the conductive posts 210 and the conductive segments 220 have been fabricated and interconnected to form the conductive coil 230. FIG. 8B illustrates a top view of the substrate 110 shown in FIG. 8A.

FIG. 8C illustrates a cross-sectional view of the substrate 110 along the line 8C—8C shown in FIG. 8A. As discussed above with respect to FIGS. 5A–5C, those of ordinary skill in the art will understand that the conductive posts 210 and the conductive segments 220 can be fabricated from a wide variety of suitable conductive materials, such as metals (e.g., aluminum, copper, gold, and the like), alloys, doped polysilicon, metal silicides, and the like. In general, materials having a higher conductivity are preferred to materials having a lower conductivity.

In one embodiment, the conductive material is used to fill or partially fill the paths 140 to form the plurality of conductive posts 210. In an alternative embodiment, the conductive coil 230 is partially diffused into the substrate 110.

In one embodiment, each conductive post 210 and conductive segment 220 is fabricated from a different conductive material. This configuration is particularly advantageous because the properties of the conductive coil 230 can be easily tuned through the selection of the various conductive materials. For example, the internal resistance of the conductive coil 230 can be increased by selecting a material having a higher resistance for a particular conductive segment 220 than the average resistance in the rest of the conductive coil 230.

In another embodiment, two different conductive materials are selected for fabricating the conductive coil 230. In this embodiment, materials are selected based on their compatibility with the available integrated circuit manufacturing processes. For example, if it is difficult to create a barrier layer where the conductive coil 230 pierces the substrate 110, then the conductive posts 210 that pierce the substrate 110 can be fabricated from aluminum. On the other hand, if it is relatively easy to create a barrier layer for the conductive segments 220 that interconnect the conductive posts 210, then copper can be used for the conductive segments 220.

FIG. 9A illustrates an isometric view of an inductor 100 in accordance with the present invention after the formation of two passivation layers 500 around the conductive coil 230. FIG. 9B illustrates a top view of the inductor 100 shown in FIG. 9A. FIG. 9C illustrates a cross-sectional view of the inductor 100 along the line 9C—9C shown in FIG. 9A. As illustrated, the passivation layers 500 are formed on the top surface 120 and on the bottom surface 130 of the substrate 110. The passivation layers 500 advantageously protect the exposed portions of the conductive coil 230 from moisture, contamination, and physical damage. In addition, the passivation layers 500 electrically isolate the conductive coil 230 from any conducting layers deposited above the conductive coil 230.

Those of ordinary skill in the art will understand that the passivation layers 500 may comprise a variety of suitable nonconductive materials. The particular material for the passivation layers 500 can advantageously be selected based upon the thermal budget requirement. For low-temperature processing, for example, the passivation layers 500 may comprise polymers such as Parylene and polyimide. For ordinary processing at high temperature, on the other hand, the passivation layers 500 may comprise inorganic oxide such as silicon dioxide, nitride, or the combination of these.

FIG. 10 illustrates a top view of one embodiment of an inductor-coupled circuit 600 in accordance with the present invention. The inductor-coupled circuit 600 comprises an inductor 100 and a circuit 610 formed on a substrate 110. Those of ordinary skill in the art will understand that the

circuit 610 can comprise a wide variety of suitable electronic circuits. In one embodiment, for example, the circuit 610 comprises a plurality of memory cells. The inductor 100 can be fabricated using any of the processes described above or using any other suitable process. The inductor 100 is electrically coupled to the circuit 610 by a plurality of conductive paths 620 formed on the substrate 110. Those of ordinary skill in the art will understand that the conductive paths 620 can be formed from a variety of conductive materials and using any of variety of well-known methods.

FIG. 11 illustrates a block diagram of a system level embodiment of the present invention. A system 700 comprises a processor 705 and a memory device 710, which includes memory circuits and cells, electronic circuits, electronic devices, and a power supply circuit 712 coupled to a plurality of inductors 100 of one or more of the types described above. The memory device 710 comprises a memory array 715, address circuitry 720, and read circuitry 730. Furthermore, the memory device 710 is coupled to the processor 705 by an address bus 735, a data bus 740, and a control bus 745.

The processor 705, through the address bus 735, the data bus 740, and the control bus 745, communicates with the memory device 710. In a read operation initiated by the processor 705, address information, data information, and control information are provided to the memory device 710 through the address bus 735, the data bus 740, and the control bus 745, respectively. This information is decoded by addressing circuitry 720, which includes a row decoder and a column decoder, and read circuitry 730. Successful completion of the read operation results in information from the memory array 715 being communicated to the processor 705 over the data bus 740.

Although the foregoing has been a description and illustration of specific embodiments of the invention, various modifications and changes can be made thereto by persons skilled in the art, without departing from the scope and spirit of the invention as defined by the following claims.

What is claimed is:

1. An inductor comprising:

a substrate;

a magnetic core embedded within said substrate; and

a three-dimensional conductive coil comprising a plurality of conductive posts interconnected by a plurality of conductive segments,

wherein said conductive coil surrounds said magnetic core, and

wherein said magnetic core comprises a porous region of said substrate having a ferromagnetic material deposited therein.

2. The inductor of claim 1, wherein said substrate comprises silicon carbide.

3. The inductor of claim 1, wherein each of said plurality of conductive posts and said plurality of conductive segments is fabricated from a different conductive material.

4. The inductor of claim 1, wherein each of said plurality of conductive posts and said plurality of conductive segments is fabricated from one of two different metals.

5. A method of fabricating an inductor embedded in a substrate, said method comprising the steps of:

forming a plurality of paths extending through said substrate;

forming a magnetic core in said substrate;

depositing a conductive material in said paths to form a plurality of conductive posts; and

fabricating a plurality of conductive segments that interconnect said conductive posts to form a conductive coil,

wherein said step of forming a magnetic core comprises:

forming a porous region in said substrate; and

depositing a ferromagnetic material in said porous region.

6. The method of claim 5, wherein said step of forming a plurality of paths comprises forming two substantially parallel rows of paths extending through said substrate.

7. The method of claim 5, wherein said step of forming a plurality of paths comprises using an etching process.

8. The method of claim 5, wherein said step of forming a plurality of paths comprises using a laser.

9. The method of claim 5, wherein said step of forming a plurality of paths comprises using a drill.

10. The method of claim 5, wherein said step of forming a magnetic core comprises forming a magnetic core in a region of said substrate bounded by said plurality of paths.

11. The method of claim 5, wherein said step of forming a porous region comprises using an anodic etching process.

12. The method of claim 5, wherein said step of forming a porous region comprises using a laser ablation process.

13. The method of claim 5, wherein said step of depositing a ferromagnetic material comprises depositing Permalloy.

14. The method of claim 5, wherein said step of depositing a ferromagnetic material comprises using a chemical vapor deposition process.

15. The method of claim 5, wherein said step of depositing a conductive material in said paths comprises one of filling or lining said paths with said conductive material.

* * * * *

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United States Patent [19]

Burghartz et al.

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[45] Date of Patent: Mar. 23, 1999

[54] **INTEGRATED CIRCUIT INDUCTOR**

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Related U.S. Application Data

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[51] Int. Cl.[6] H01F 5/00; H01F 27/28; H01F 7/06

[52] U.S. Cl. 336/200; 336/232; 336/223; 29/602.1

[58] Field of Search 336/200, 229, 336/223, 232

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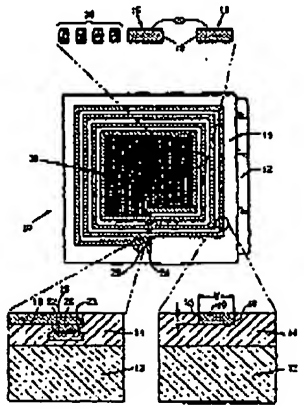
[57] ABSTRACT

High quality factor (Q) spiral and toroidal inductor and transformer are disclosed that are compatible with silicon very large scale integration (VLSI) processing, consume a small IC area, and operate at high frequencies. The spiral inductor has a spiral metal coil deposited in a trench formed in a dielectric layer over a substrate. The metal coil is enclosed in ferromagnetic liner and cap layers, and is connected to an underpass contact through a metal filled via in the dielectric layer. The spiral inductor also includes ferromagnetic cores lines surrounded by the metal spiral coil. A spiral transformer is formed by vertically stacking two spiral inductors, or placing them side-by-side over a ferromagnetic bridge formed below the metal coils and cores lines. The toroidal inductor includes a toroidal metal coil with a core having ferromagnetic strips. The toroidal metal coil is segmented into two coils each having a pair of ports to form a toroidal transformer.

4 Claims, 5 Drawing Sheets



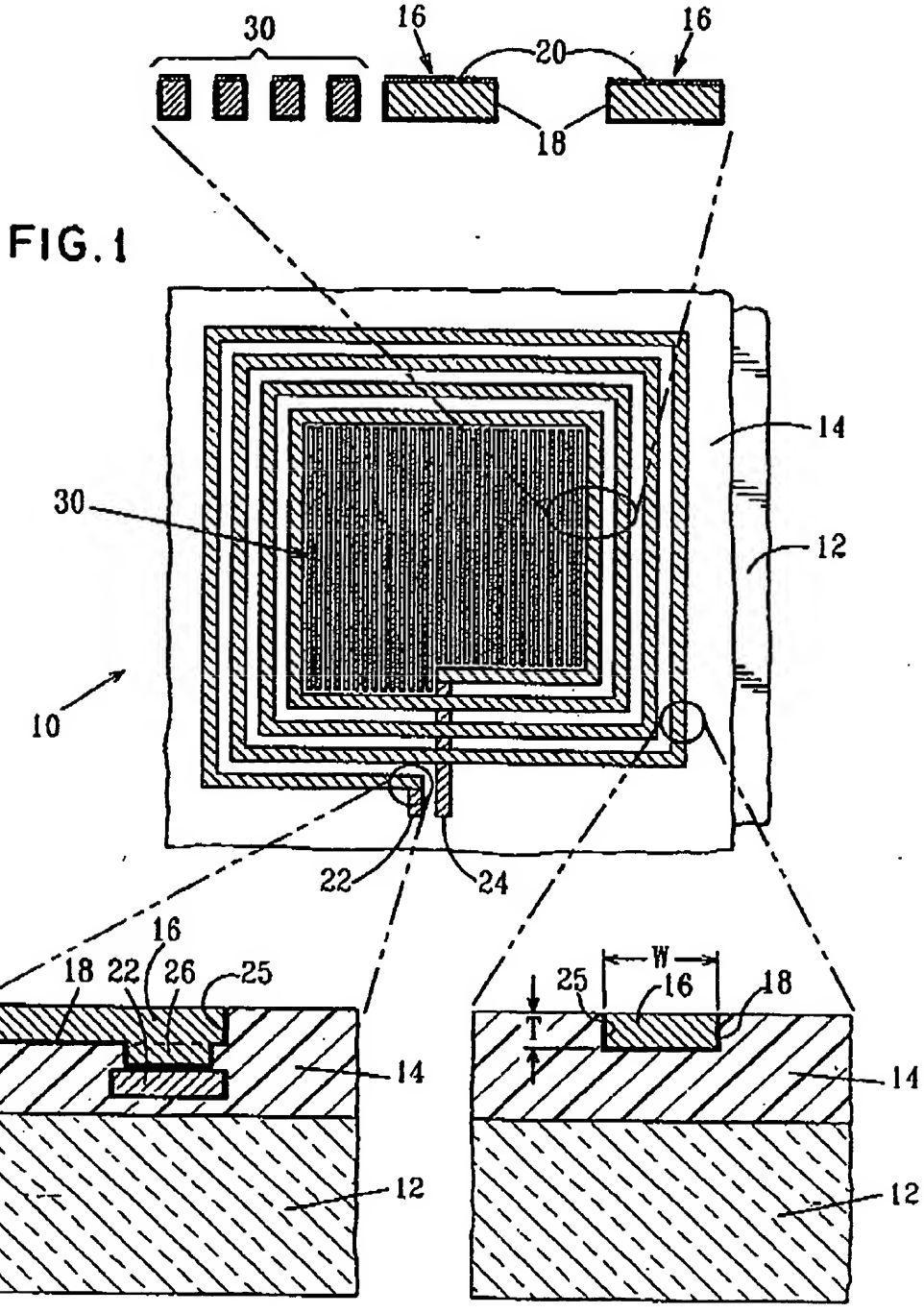
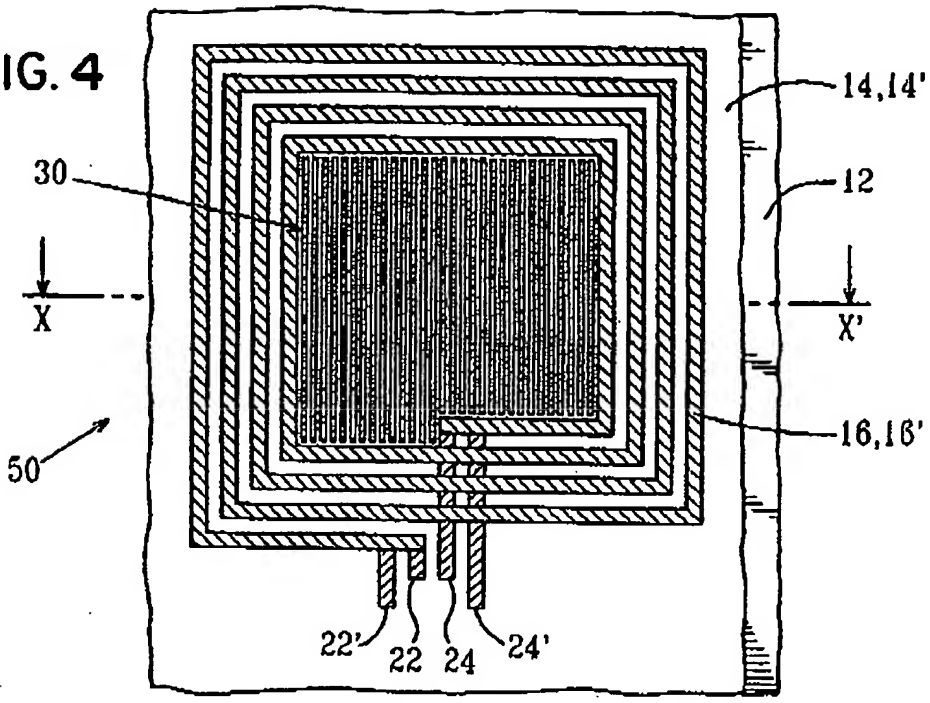


FIG. 1

FIG. 2

FIG. 3

FIG. 4



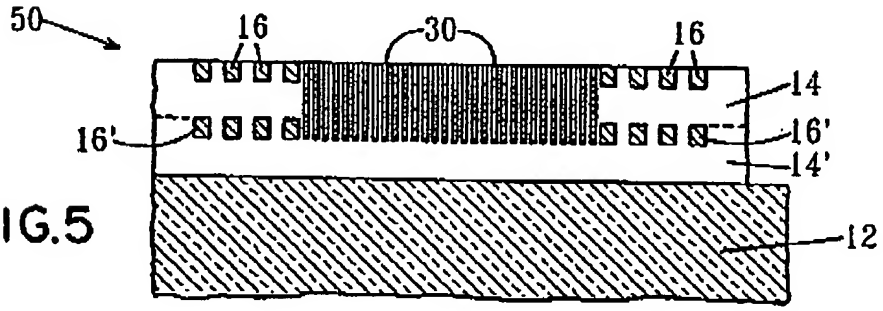
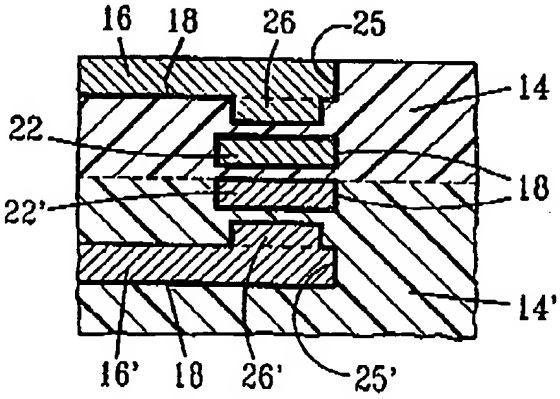


FIG.5

FIG. 6



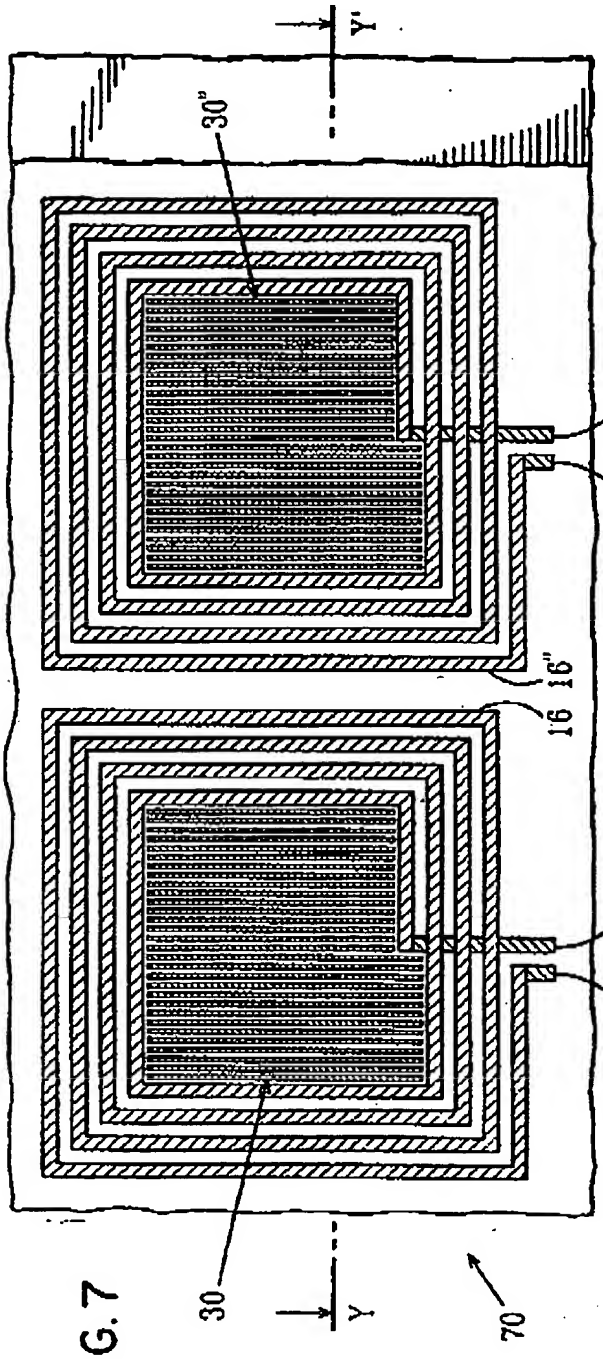


FIG. 7

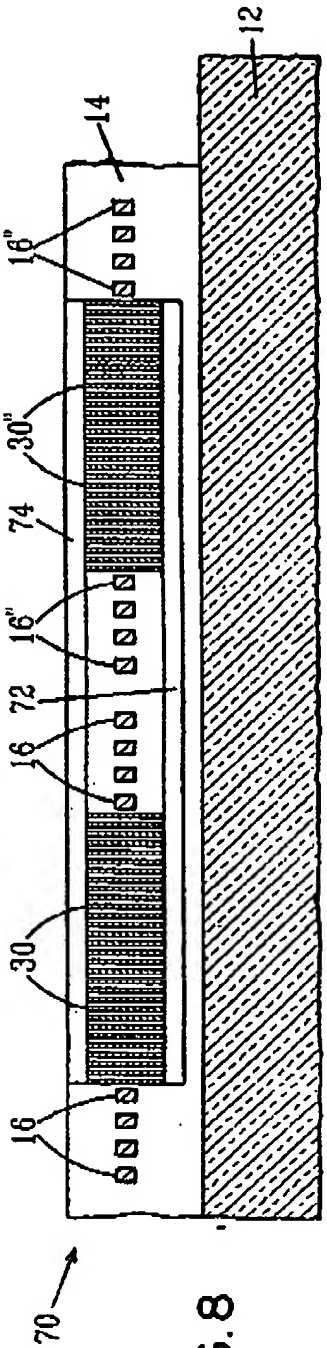


FIG. 8

FIG.9

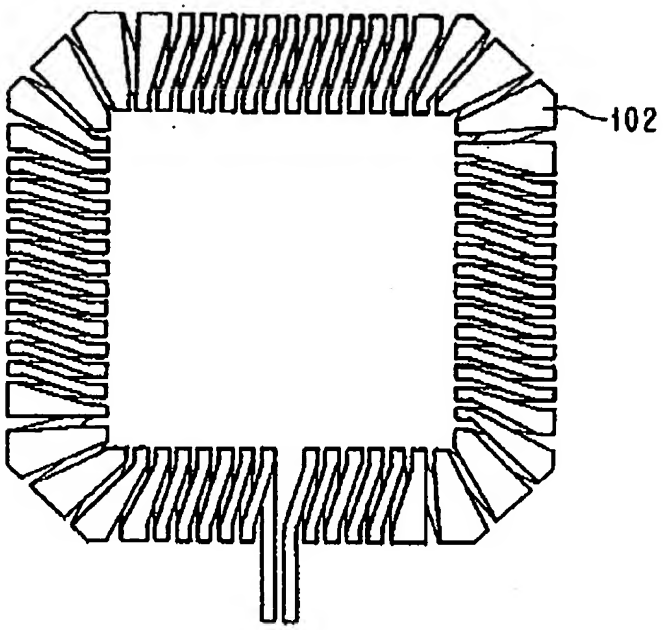
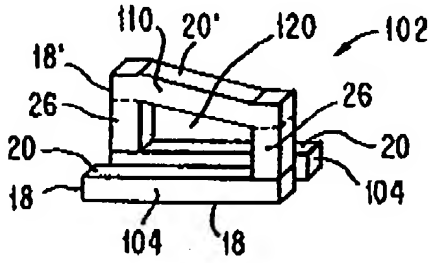


FIG. 10



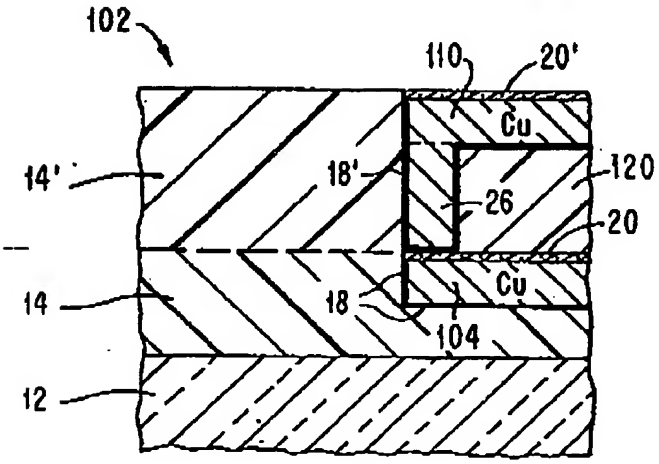


FIG. 11

FIG. 12

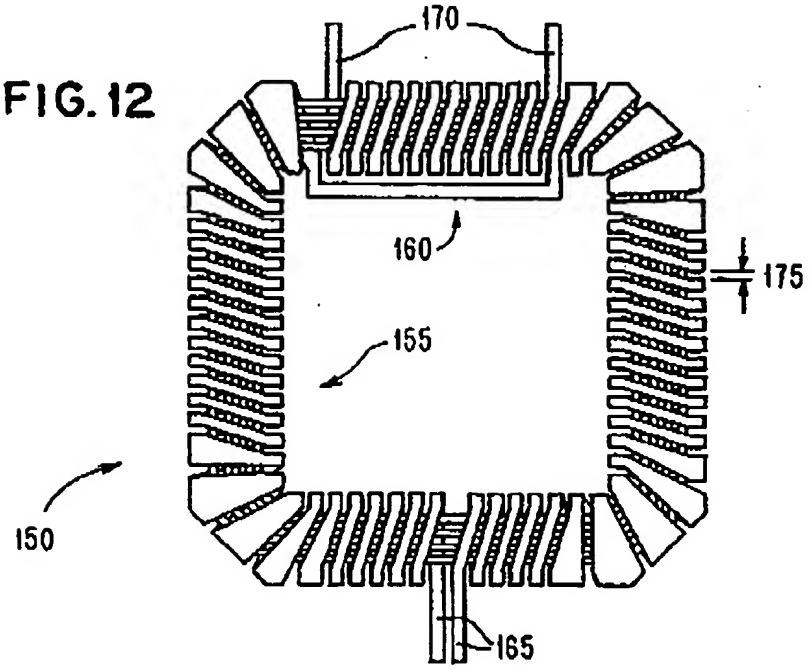
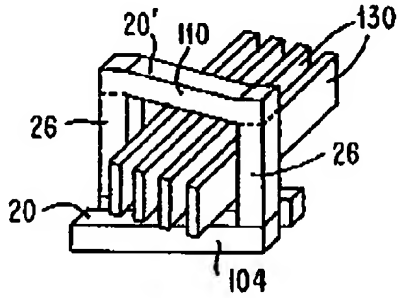


FIG. 13



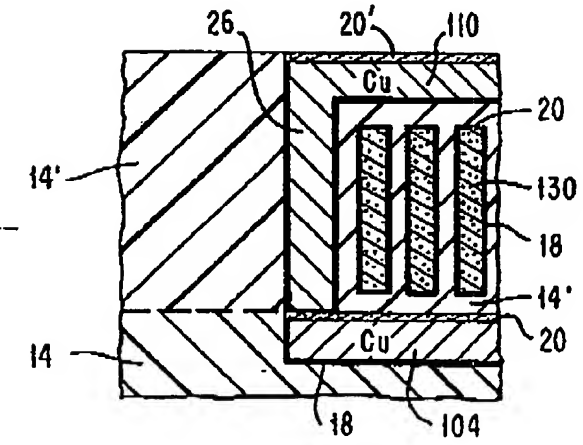


FIG. 14.

INTEGRATED CIRCUIT INDUCTOR

This application is a division of application Ser. No. 08/701,922 filed Aug. 23, 1996 which application is now allowed.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is directed to integrated circuit inductors and transformers, and methods for making thereof, and more particularly, to spiral and toroidal inductors and transformers having high quality factor Q.

2. Discussion of the Prior Art

Many digital and analog components and circuits have been successfully implemented in silicon (Si) based integrated circuits (ICs). Such components include passive devices, such as resistors, capacitors, and inductors.

Implementing high quality factor (Q) inductors that operate at high radio frequencies (RFs) remain problematic in silicon based very large scale integration (VLSI) IC semiconductor chips. For microwave and wireless communications applications, it is desirable to integrate inductors and transformers monolithically on bulk silicon (Si), silicon-on-insulator (SOI), or silicon-on-sapphire (SOS) chips. For these applications, considerable innovation is necessary before adequate values of inductance (L), as well as high quality-factor (Q), are obtained. The quality-factor (Q) is given by equation (1):

$$Q=\omega_0 L/R \quad (1)$$

where,

ω_0=center or resonant angular frequency of oscillation;

L=inductance; and

R=resistance.

Most structures and methods used for fabricating high Q inductors and transformers in hybrid circuits, monolithic microwave integrated circuits (MMICs), or discrete applications (e.g., at larger dimensions, with better metals, on lossless substrates, etc.) are not readily compatible with silicon VLSI processing. The following references discuss conventional high Q inductor fabrication methods:

1. R. Naster et al., "Method for Fabricating Silicon-on-Sapphire Monolithic Microwave Integrated Circuits", U.S. Pat. No. 4,418,470 (1983);
2. R. Stengel and C. Nejdl, "Planar Inductors", U.S. Pat. No. 4,494,100 (1985);
3. R. Scranton and D. Thompson, "Capacitive Sensing Employing Thin Film Inductors", U.S. Pat. No. 4,648,087 (1987);
4. J. Bhagat, "Miniature Inductor for Integrated Circuits and Devices", U.S. Pat. No. 5,070,317 (1991);
5. N. Andob et al., "Inductive Structures for Semiconductor Integrated Circuits", U.S. Pat. No. 5,095,357 (1992);
6. A. Hubbard, "Integrated Circuit Inductor", U.S. Pat. No. 5,227,659 (1993);
7. L. Saadat and M. Thomas, "Process for Making Microcomponents Integrated Circuits", U.S. Pat. No. 5,279,988 (1994); and
8. C. Ahn et al., "A Fully Integrated Planar Toroidal Inductor with a Micromachined Nickel Iron Magnetic Bar", IEEE Trans. Compon. Packag. Manuf. Technol. A 17,463 (1994).

Conventional inductors and transformers on silicon, which have strictly planar structures and are fabricated with conventional silicon fabrication processes and material, suffer from several limitations. First, conventional aluminum interconnect technology has a relatively high metal resistivity and limited metal thickness, both of which lead to a relatively high resistance of the spiral coil. The high resistivity R lowers the quality factor Q, as seen from equation (1). Second, magnetic fields are strongly coupled to the Si substrate, which is a lossy conductor with large skin depth. Induced currents in the Si substrate act to oppose those in the spiral coil of the inductor and thus reduce the inductance L. Furthermore, energy is dissipated by the high resistivity of the Si substrate, which further decreases the quality-factor Q.

To date, Q values for inductors made by conventional methods are significantly below those achievable on a printed circuit board, or on gallium arsenide (GaAs) substrates with gold (Au) metalization. Another problem is that high inductance values (L), as are required in RF chokes for example, require a large silicon chip area. The large area requirement prevents miniaturization of chips. In addition, physically large RF chokes cannot operate at high frequencies, where the short wavelengths necessitates physically small and miniature components.

To overcome some of the limitations of spiral inductors, toroidal inductors are used. Conventional multilevel interconnect technology allows fabrication of solenoidal or toroidal inductor structures instead of an inductor having a spiral configuration. Toroidal inductors have the benefit of confining the magnetic flux, thereby minimizing substrate losses. However, conventional integrated toroidal inductors have comparably small inductance and Q values for a given silicon area, relative to the planar spiral inductor configuration. This is because the area enclosed by wire windings of conventional toroidal inductors is small due to the limit in vertical dimensions of the thin films used in conventional VLSI processing.

In light of the foregoing, there is a need for high Q inductors and transformers suitable for integration in IC chips, such as VLSI IC chips.

SUMMARY OF THE INVENTION

The object of the present invention is to provide high Q inductors and transformers, and methods of making thereof, that eliminate the problems of conventional inductors and transformers.

Another object of the present invention is to provide high Q inductors and transformers that are suitable for integration in VLSI IC chips, consume a small IC area, and operate at high frequencies.

These and other objects of the inventions are achieved by a spiral inductor and a method of making thereof. The spiral inductor comprises a substrate; a dielectric layer having a spiral trench; and a first spiral metal coil formed in the spiral trench over the liner to increase an aspect ratio thereof.

A ferromagnetic liner lines the bottom and sides of the trench, and a cap layer may cap the first metal coil so that the first spiral metal coil is enclosed by the cap and liner layers. In addition, an underpass contact is formed in the dielectric layer below one end of the first metal coil. This one end of the first metal coil extends into a via formed in the dielectric layer to connect to the underpass contact.

Ferromagnetic core lines are formed in a core surrounded by the first metal coil. These core lines are electrically separated from each other.

In another embodiment of the present inventions, a second metal coil is formed in the dielectric layer. The second metal coil may be vertically stacked over the first metal coil or adjacent thereto. In the latter case, a ferromagnetic bridge is formed below, and contacts, the two adjacent metal coils. The ferromagnetic bridge may also be formed below the first metal coil in the vertically stacked coils configuration. The ferromagnetic bridge reduces magnetic flux penetration into the substrate. This increases the quality factor Q by increasing the inductance L.

In the vertically stacked configuration, an overpass contact may be formed in the dielectric layer above the second metal coil. The two vertically stacked or adjacent coils may each have a pair of ports to form a spiral transformer.

Another embodiment of the present inventions is a toroidal inductor and a method of making thereof. The toroidal inductor comprises a dielectric layer formed over a substrate, and a toroidal metal coil formed in the dielectric layer.

The toroidal metal coil is formed by segmenting the first metal coil of the spiral inductor into first metal segments that are electrically separated from each other by the dielectric layer. Second metal segments are formed over the first metal segments, where the second metal segments are electrically separated from each other and from the first metal segments by the dielectric layer. Metal studs are formed in the dielectric layer to connect opposing ends of the two metal segments to form the toroidal metal coil in the dielectric layer.

Inner and outer surfaces of the toroidal metal coil are lined with a ferromagnetic material. Ferromagnetic material or strips are formed in a core defined by the inner surface of the toroidal metal coil. The ferromagnetic strips are separated from each other and from the inner surface by the dielectric layer.

The spiral and toroidal inductors are formed using a series of damascene processes, as described in greater detail in U.S. Pat. Nos. 4,702,792 and 4,789,648, both to Chow et al., and U.S. Pat. No. 4,944,836 to Beyer et al., all assigned to IBM corporation and incorporated herein by reference. These damascene processes include etching trenches in the dielectric, filling the trenches with desired material, e.g., metal or ferromagnetic, and planarizing to remove excess material remaining after the filling step.

The integrated spiral transformer on a silicon substrate, which is formed by coordinating two spiral coils or inductors in a vertically stacked or side-by-side structure, has undesirable capacitive coupling. That is, coupling between two ports of the spiral transformer, made from two spiral inductors, is not only of an electromagnetic type, as desired. In addition to the electromagnetic component of the coupling between the two spiral transformer ports, there is also a strong capacitive component as a result of the geometrical arrangement.

To reduce the capacitive coupling, another embodiment of the present invention, is an integrated toroidal transformer on a silicon substrate. A toroidal transformer is formed by splitting or segmenting the toroidal coil of the toroidal inductor into two separate windings or coils, each having a pair of ports. This forms the toroidal transformer that has a much less undesirable capacitive cross-coupling than the spiral transformer.

The inventive inductor structure includes single-and multilevel integrated inductor structures made by a metal (single) damascene and dual-damascene processes, for example, with copper as the metal. Optional ferromagnetic thin-film materials may be used. The inventive inductor is easily incorporated on VLSI integrated circuit (IC) chips.

Advantages of the inventive inductor include the following. First, use of the damascene and dual-damascene processes, with a preferred (high-conductivity) metal such as copper (gold or silver), allow thicker dimensions for single and multilevel interconnects. The thick interconnects further lower the interconnect resistance. The thick interconnects, and the low resistance material (e.g., copper), greatly reduce inductor parasitic resistance R, thereby increasing Q.

Second, a ferromagnetic liner near sidewalls, bottoms, and/or tops of a metal line or coil of the inductor, e.g., the spiral inductor, as can readily be incorporated by the damascene process, increases the permeability in the region enclosed by the inductor where the magnetic field is the largest. This increases the inductance L, which in turn increases Q.

Third, a further increase of L is achieved by adding laminated dummy structures of ferromagnetic and copper material in a central or core region of the inductor structure. The ferromagnetic core is also beneficial in a transformer structure, comprising two or more vertically stacked or side-by-side spiral coils, because the ferromagnetic core increases the mutual inductance between the coils without increasing the parasitic capacitance.

Fourth, a ferromagnetic core can also be introduced into the toroidal inductor structure so that the inductance is increased significantly over that achievable with an air core. A toroidal transformer with a ferromagnetic core has the advantage that the coils could be spaced apart laterally, in order to reduce the parasitic capacitance between them, without sacrificing mutual inductive coupling.

BRIEF DESCRIPTION OF THE DRAWINGS

Further features and advantages of the invention will become more readily apparent from a consideration of the following detailed description set forth with reference to the accompanying drawings, which specify and show preferred embodiments of the invention, wherein like elements are designated by identical references throughout the drawings; and in which:

FIGS. 1–3 show top and cross-sectional views of a damascene spiral inductor according to the present invention;

FIGS. 4–6 show top and cross-sectional views of a damascene spiral transformer having vertically stacked spiral coils according to the present invention;

FIGS. 7–8 show top and cross-sectional views of a damascene spiral transformer having side-by-side spiral coils according to the present invention;

FIGS. 9–11 show top, partial three-dimensional, and cross-sectional views of a damascene toroidal inductor with an air core according to the present invention; and

FIGS. 12–14 show top, partial three-dimensional, and cross-sectional views of a damascene toroidal transformer with a ferromagnetic core according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGS. 1–3 show top and cross-sectional views of a damascene copper/ferromagnetic spiral VLSI inductor 10, according to one embodiment of the present invention. The spiral inductor 10 is fabricated over a substrate 12, which may be silicon (Si), silicon-on-insulator (SOI), or silicon-

on-sapphire (SOS), for example. A dielectric layer or film 14 is formed over the substrate 12. The substrate 12 is separated from a metal line or coil 16 by the dielectric film 14. Illustratively, the metal 16 is copper (Cu), aluminum (Al), tin (Ti), gold (Au), silver (Ag), or a combined alloy thereof. Preferably, the metal 16 is copper. The metal line 16 is arranged in a spiral shape. FIG. 1 shows the metal line 16 in a square spiral shape, however, other spiral shapes, such as rectangular or circular spirals may also be formed.

The metal line 16 is formed by using a dual damascene process, which includes the following steps:

(a) etching a spiral trench 25 and via 26 into the dielectric film 14;

(b) depositing metal 16 in the etched spiral trench 25; and

(c) planarizing, e.g., chemical-mechanical polishing (CMP), the deposited metal 16 to remove excess metal from the wafer surface.

The metal depositing step comprises electrolytic or electroless plating of a high conductivity metal, such as copper, gold, and silver, for example. Alternatively, the metal depositing step comprises chemical vapor deposition of a high conductivity metal, such as aluminum for example.

A single damascene process refers to forming and filling trenches, while a dual damascene process refers to simultaneously forming trenches and vias, and filling thereof with a desired material.

The trench 25 fabricated by the dual damascene process, and consequently the metal line 16 filling the trench 25, have a large aspect ratio. The aspect ratio of the metal line 16 is the ratio of thickness to width T/W of the metal line 16 where T is thickness and W is width. The metal line 16 formed by this damascene process is thick, thus having an increased aspect ratio. This reduces the resistance of the metal line or coil 16, which increases the quality factor Q. Illustratively, the thickness T of the metal line 16 is approximately 3 microns, and the width W is approximately 3 microns or more.

The Cu-dual-damascene process enables substantial series-resistance reduction compared to Al(Cu)Ti wiring (e.g. 3×reduction). This is due to an approximately 40% resistance reduction of copper and the larger aspect ratios achieved with the damascene process.

Further, this damascene process allows addition of a liner film 18 prior to metal 16 deposition step (b). The liner film 18 lines the bottom and sidewalls of the trench, and separates the metal line 16 from the dielectric layer 14. The inductance (L) per line length of the spiral inductor 10 is increased by using a ferromagnetic material, such as Permalloy, AlNiCo, etc., for the liner film 18.

Next, a cap layer 20 (FIG. 1), which may be of the same ferromagnetic material as the liner 18, is formed over the top of the metal line 16. This encloses the metal line 16 by the ferromagnetic material of the liner 18 and cap 20. Illustratively, the cap layer 20 is formed by electroless plating. The ferromagnetic liner and cap 18, 20 increase the self-inductance of the wire 16, thus increasing the total inductance L.

The dual-damascene process is also used for the formation of underpass contacts 22, 24 at the ends of the spiral metal line 16. The underpass contacts 22, 24 are located below the metal line 16, and are connected to the ends of the spiral metal line 16 through metal filled vias, one of which is shown in FIG. 2 as reference number 26. Illustratively, the underpass contacts 22, 24 are perpendicular to the metal line 16.

Forming the underpass contacts 22, 24 and vias 26 by this dual-damascene process has the advantage that the same

metal deposition and CMP steps simultaneously form both the via 26 and the metal line 16. A single damascene process may also be used instead of the dual-damascene process, to form the spiral metal coil 16 over a preformed via 26 and underpass contacts 22, 24.

The copper damascene process in particular enables formation of much higher aspect-ratio lines and much larger-area vias than conventional Al-line/W-stud processes. The large aspect ratio of the metal line 18 substantially reduces the series-resistance of the spiral inductor 10. Similarly, the larger-area vias 22, which are filled with a metal having a low resistance, substantially reduce the contact and via resistances in the multiple-level spiral inductor 10.

A core comprising narrow dummy-lines 30 may be added to the center region of the spiral inductor surrounded by the metal line 16, without using any additional process steps. For example, during the dielectric 14 etching step, trenches are formed therein for both the metal line 16 and the ferromagnetic core lines 30.

The step of depositing the ferromagnetic liner in the spiral trench to be filled with the metal coil 16 also fills the core trenches to form the ferromagnetic core lines 30.

Illustratively, these core trenches are narrow and parallel to each other. The core trenches are narrow so that they become nearly completely filled during the ferromagnetic liner film deposition step. This maximizes the permeability of the core trenches. Thus volume-fraction, or the percent volume of the ferromagnetic material relative to the available volume, is high in the core lines 30, and low in the much wider spiral metal line windings 18, contact via 26, and underpass 22. This minimizes the series resistance of the inductor windings. The core lines 30 are also separated electrically by the dielectric layer 14, e.g., laminated, so that Eddy currents cannot flow in the core lines 30.

As shown in FIGS. 4–6, in another embodiment of the present invention, two spiral coils or metal lines 16, 16' are vertically stacked over each other to form a spiral transformer 50. The spiral transformer 50 has a pair of ports or contacts 22, 24, and 22', 24', associated with the spiral metal lines 16, 16', respectively. FIG. 5 is the cross-sectional view of FIG. 4 along lines XX'. FIG. 6 is the cross-sectional view of contact regions of FIG. 4 and is comparable to FIG. 2.

Many features of the spiral transformer 50 are similar to that of the spiral inductor 10. That is, each of the two spiral coils 16, 16' is formed by using similar steps which form similar elements 16–26 shown in FIGS. 1–3. As shown in FIG. 6, the only difference is that element 22' refers to an overpass contact 24', instead of the underpass contact 22, and via 26' is located below the overpass contact 22' of the lower metal lines 16', as compared to the via 26, which is located above the underpass contact 22.

In an illustrative embodiment, after forming a first metal coil 16' in a first spiral trench 25' etched in a first dielectric layer 14', a second metal coil 16 is formed in a second spiral trench 25 etched in a second dielectric layer 14. The second metal coil 16 is vertically stacked over and electrically separated, by the dielectric layer 14, from the first metal coil 16'.

As in the spiral inductor 10 of FIGS. 1–3, ferromagnetic core lines 30, which are parallel to each other for example, are formed in the dielectric layer 14 in a core surrounded by the vertically stacked spiral coils 16, 16'. The ferromagnetic core lines 30 improve electromagnetic coupling between the vertically stacked spiral coils 16, 16' in the spiral transformer structure 50, which is integrated on the substrate 12. The ferromagnetic core lines 30 of the spiral transformer 50 extend from the top surface of the transformer 50 to reach a

depth in the dielectric layer 14, which depth is similar to the depth of the lower elements 16' to 26'.

FIGS. 7–8 show an alternative embodiment of a spiral transformer 70, comprising two spiral inductors 10 of FIGS. 1–3 formed side-by-side, e.g., either concurrently or sequentially, over the substrate 12. FIG. 7 is a top view of the spiral transformer 70, while FIG. 8 is a cross-sectional view of FIG. 7 along line YY'. The side-by-side spiral coils 16, 16" of the transformer 70 surround ferromagnetic cores 30, 30", respectively. In this case, both spiral coils 16, 16" are preferably contacted through underpass contacts, which are similar to the underpass contact 22 shown in FIG. 2. A ferromagnetic bridge 72 is formed during the fabrication process of those underpass contacts. The ferromagnetic bridge 72 is formed below and between adjacent portions of the two spiral coils 16, 16", and below the two ferromagnetic core lines 30, 30". The ferromagnetic bridge 72 increases the mutual inductance between the two spiral coils 16, 16".

A second ferromagnetic bridge 74 may be provided to further increase the mutual inductance between the two spiral coils 16, 16". The second ferromagnetic bridge 74 may be formed over the two spiral coils 16, 16" and ferromagnetic core lines 30, 30", for example, aligned with the lower ferromagnetic bridge 72. By confining large portions of the magnetic fields external to the two spiral coils 16, 16", these ferromagnetic bridges 72, 74 decouple the transformer from the integrated circuit substrate. Such a ferromagnetic bridge structure can also be applied to the stacked transformer structure 50 of FIGS. 4 and 5 and to the spiral inductor 10 of FIGS. 1–3 in order to reduce or restrain the magnetic flux from entering the lossy silicon substrate.

In another embodiment of the present invention, toroidal inductor and transformer structures are formed by using a similar fabrication process as described in connection with the spiral inductor 10 and transformers 50, 70 of FIGS. 1–8. FIG. 9 shows a top view of a damascene toroidal inductor 100 having continuous loops 102 that are arranged to form a square shaped toroidal inductor 100. The loops 102 may also be arranged to form other shaped toroidal inductors, such as rectangular or circular toroidal inductors. FIG. 10 shows a three-dimensional perspective view of one of the loops 102, and FIG. 11 shows a cross-sectional view of a partial loop 102.

As shown in FIGS. 10 and 11, the loop 102 has first or lower metal, e.g., copper (Cu), sections 104 that are separated from each other. The lower Cu sections 104 are formed using a process similar to that described in connection with FIG. 3. That is, a planar spiral trench is formed, e.g., etched, in the dielectric layer 14, and metal deposited therein. Next, the planar spiral metal is segmented, e.g., portions thereof etched, to form the separated metal segments or sections 104.

Preferably, instead of forming a single planar spiral trench, separated trenches are formed on the dielectric layer 14 located above the substrate 12, and are arranged adjacent to each other to form a planar loop having a square, rectangular, circular or other shapes. The trenches are filled with copper 104. Excess copper is removed by planarizing, e.g., using CMP.

Similar to FIG. 3, a ferromagnetic liner 18 may be formed at bottom and sides of the trenches prior to deposition of the metal. The ferromagnetic liner 18 enhances the inductance of the metal sections 104. A ferromagnetic cap 20 may also be formed over the metal sections 104. This encloses the metal sections 104 with the ferromagnetic liner 18 and caps 20.

Next another dielectric layer 14' is deposited over the capped metal sections 104 and exposed portions of the first or lower dielectric layer 14. A dual-damascene Cu-process is used to form vias 26 and a set of top trenches by selectively etching the top dielectric layer 14'. Each vias 26 extends to one end of the lower metal sections 104. A separate via 26 is formed over each end of each lower metal section 104.

The dual damascene process also includes filling the vias 26 and top trenches with metal. The deposited copper in the top trenches forms the top Cu sections 110. Filling the vias 26 and top trenches with metal forms the toroidal coil loops 102 having lower and upper metal sections 104, 110, and vias 26. Each toroidal coil loop 102 has its top Cu section 110 connected to an opposite end of an adjacent lower Cu sections 104. Inner surfaces of the toroidal coil loops 102 define a core 120.

Prior to this deposition of metal, the vias 26 and top trenches may be lined with a ferromagnetic liner 18'. A ferromagnetic cap 20' may also be formed over the top Cu sections. This encloses the top Cu sections 110 in ferromagnetic material.

Instead of having a dielectric core 120 between two Cu sections 104, 110 and vias 26, ferromagnetic strips may be formed in the core 120. FIG. 13 shows ferromagnetic strips 130 formed within the dielectric layer of the core 120. The ferromagnetic strips 130 are preferably formed using a damascene process and do not electrically contact the metal sections 104, 110. Instead of the ferromagnetic strips 130, a ferromagnetic layer electrically insulated from the metal section 104, 110 may be formed, by the damascene process. However, segmenting the ferromagnetic layer into the ferromagnetic strip 130 prevents excessive Eddy currents.

The damascene process forming the ferromagnetic layer or ferromagnetic strips is similar to previously described damascene processes. That is, the top dielectric layer 14' is formed over the lower as sections 104, trenches etched therein and lined with ferromagnetic liner 18. Next, ferromagnetic material is deposited to fill the lined trenches. Excess ferromagnetic material may be removed by planarizing, e.g., using CMP, and the ferromagnetic filled trenches capped with a ferromagnetic cap 20. The ferromagnetic liner 18, cap 5 and ferromagnetic material filling the trenches may be identical. That is the ferromagnetic strips 130 may be formed by filling the core trenches.

Alternatively, the ferromagnetic strips 130 may be formed as follows. After forming a thin dielectric layer over the lower Cu section 104, the ferromagnetic layer is formed in the core 120. Selectively etching the ferromagnetic layer forms the ferromagnetic strips 130 which are separated from each other.

After forming the ferromagnetic strips 130, the top dielectric layer 14' is formed thereon, (if not already present, e.g., in the case having a ferromagnetic layer instead of ferromagnetic strip 13), and using the dual-damascene Cu-process described in connection with FIGS. 10, 11, the metal filled vias 26 and top Cu sections 110 are formed to close the toroidal coil loops 102.

The toroidal inductor 100 has a larger inductance than the spiral inductor 10 of FIG. 1. The achieved inductance enhancement of the toroidal inductor 100 is roughly equal to the relative permeability of the ferromagnetic material multiplied by the volume-fraction it occupies in the core area. This inductance enhancement is in the range of approximately 500–10000. The magnetic flux is confined within the closed ferromagnetic core-loop 120 and does not stray into the silicon substrate 12, as in the case of the spiral inductor structure 10 of FIG. 1. This allows for high Q-factors at high inductance values and reduces the possibility for coupling between adjacent inductors.

The toroidal inductor 100 having a ferromagnetic core has also advantages if designed as a transformer. FIG. 12 shows a toroidal transformed 150 where the metal loops 102 of FIG. 9 are separated into two loops 155, 160, having ports 165, 170, respectively. The ferromagnetic core or strips 130 support a strong mutual inductive coupling between the ports 165, 170, while the lateral spacing 175 between adjacent loops can be sufficiently large to minimize the parasitic capacitance.

The spiral and toroidal inductors and transformers may be integrated on semiconductor integrated chips (ICs), such as VLSI chips, that include various other circuits and components, which may be active and passive devices. Illustratively, the spiral and toroidal inductors and transformers are integrated monolithically on bulk silicon (Si), silicon-on-insulator (SOI), or silicon-on-sapphire (SOS) chips. For example, such chips may operate at high radio frequencies, and used in microwave and wireless communications applications.

The inventive spiral and toroidal inductors and transformers require small silicon chip area and have thick metal coils and interconnects, i.e., metals with large aspect ratio. Thus, the metal coils and interconnects have low resistance which increases the quality factor Q. The magnetic fields are confined in the ferromagnetic strips, thus reducing coupling of the magnetic fields to the Si substrate. This increases the inductance L and, consequently, the quality factor Q. In addition, the confined magnetic fields reduce energy dissipation in the Si substrate, which prevents reduction in the quality factor Q.

The laminar ferromagnetic core lines 30 (FIG. 1) of the spiral inductor/transformer and strips 130 (FIG. 13) of the toroidal inductor/transformer further increase the inductance L, by raising the magnitude of the magnetic field in the core. In the spiral case, only a small portion of the extensive magnetic field is coupled by the ferromagnetic lines 30, increasing the inductance L by a factor of approximately 2. In the toroidal case, the ferromagnetic strip 130 increase L by up to approximately a factor of 10,000.

In a specific example, spiral inductors with Q of 40 at 5.8 GHz for a 1.4 nH inductor, and Q of 13 at 600 MHZ for an 80 nH inductor has been achieved. These inductors have approximately 2× to 3× higher Q-factors than that of conventional silicon integrated inductors.

While the invention has been particularly shown and described with respect to illustrative and preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention which should be limited only by the scope of the appended claims.

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

1. A method of forming a planar monolithic inductor comprising the steps of:

(a) forming a first dielectric layer over a substrate; and

(b) forming a toroidal metal coil in said first dielectric layer, wherein said toroidal metal coil is formed by

forming a first trench in said first dielectric layer;

depositing a first metal in said first trench; segmenting said first metal to form first metal segments;

forming a second dielectric layer over said first metal segments;

forming, in said second dielectric layer, vias over ends of said first metal segments, and a plurality of trenches between opposing vias of adjacent first metal segments; and

depositing a second metal in said plurality of trenches and vias.

2. The method of claim 1 further comprising forming ferromagnetic strips in a core defined by an inner surface of said toroidal metal coil.

3. The method of claim 1 further comprising separating said toroidal metal coil into two toroidal metal coils, each having a pair of ports to act as a toroidal transformer.

4. A method of forming a planar monolithic inductor comprising the steps of:

(a) forming a first dielectric layer over a substrate; and

(b) forming a toroidal metal coil in said first dielectric layer, wherein said toroidal metal coil is formed by

forming a first set of trenches in said first dielectric layer;

depositing a first metal in said first set of trenches to form metal segments;

forming a second dielectric layer over said metal segments;

forming, in said second dielectric layer, vias over ends of said metal segments, and a second set of trenches between opposing vias of adjacent metal segments; and

depositing a second metal in said second set of trenches and vias.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,884,990

DATED : March 23, 1999

INVENTOR(S) : Joachim N. Burghartz, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page, Section [54]: "integrated circuit inductor" should read --METHOD OF FORMING AN INTEGRATED CIRCUIT TOROIDAL INDUCTOR--

Column 1, line 1: "INTEGRATED CIRCUIT INDUCTOR" should read --METHOD OF FORMING AN INTEGRATED CIRCUIT TOROIDAL INDUCTOR--

Signed and Sealed this

Twenty-first Day of December, 1999

Attest:

Q. TODD DICKINSON

Attesting Officer

Acting Commissioner of Patents and Trademarks

US005461353A

United States Patent [19]

Eberhardt

[11] Patent Number: 5,461,353

[45] Date of Patent: Oct. 24, 1995

[54] **PRINTED CIRCUIT BOARD INDUCTOR**

[75] Inventor: John E. Eberhardt, Alpharetta, Ga.

[73] Assignee: Motorola, Inc., Schaumburg, Ill.

[21] Appl. No.: 298,497

[22] Filed: Aug. 30, 1994

[51] Int. Cl.[6] H01F 21/12; H01F 29/00

[52] U.S. Cl. ..... 333/246; 334/56; 336/84 C; 336/200

[58] Field of Search ..... 333/204, 205, 333/246; 334/56, 71; 336/200, 84 R, 84 C, 84 M, 144

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Primary Examiner—Paul Gensler

Attorney, Agent, or Firm—Pedro P. Hernandez; Kenneth M. Massaroni

[57] ABSTRACT

A multilayer printed circuit board (100) includes a plurality of layers (101, 102, 104, 106, 108 and 110). Located within intermediate layer (106) is an inductor (200) which is shielded by top layer ground plane (202) and bottom layer ground plane (204). In another embodiment of the present invention, the inductor (200) can have its inductance adjusted by way of a inductance adjustment runner (316, 318) or by an electronic inductance adjustment device (408).

11 Claims, 4 Drawing Sheets

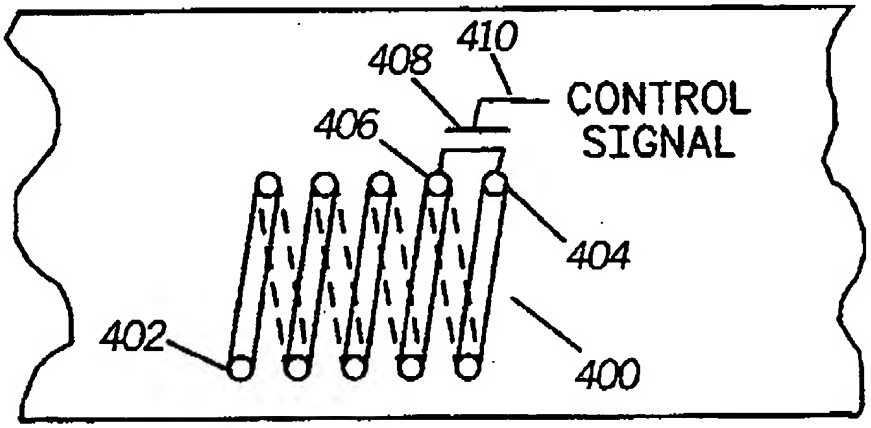

FIG.1

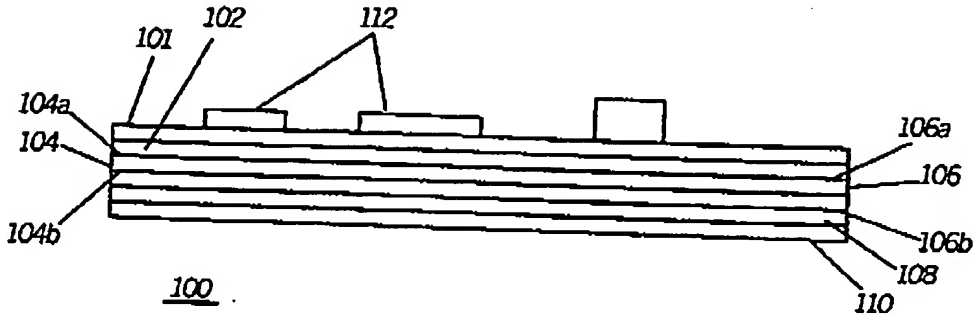

FIG.3

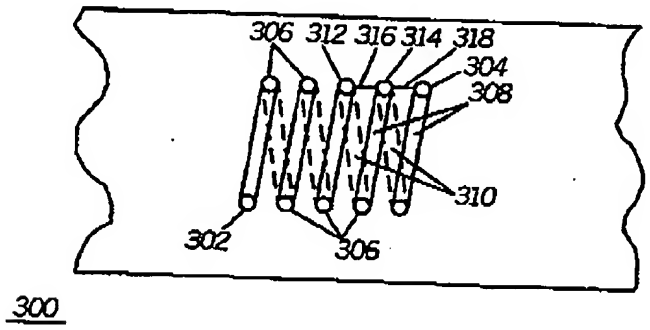

FIG.4

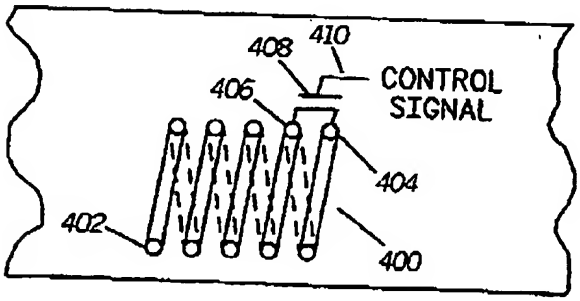

FIG.2

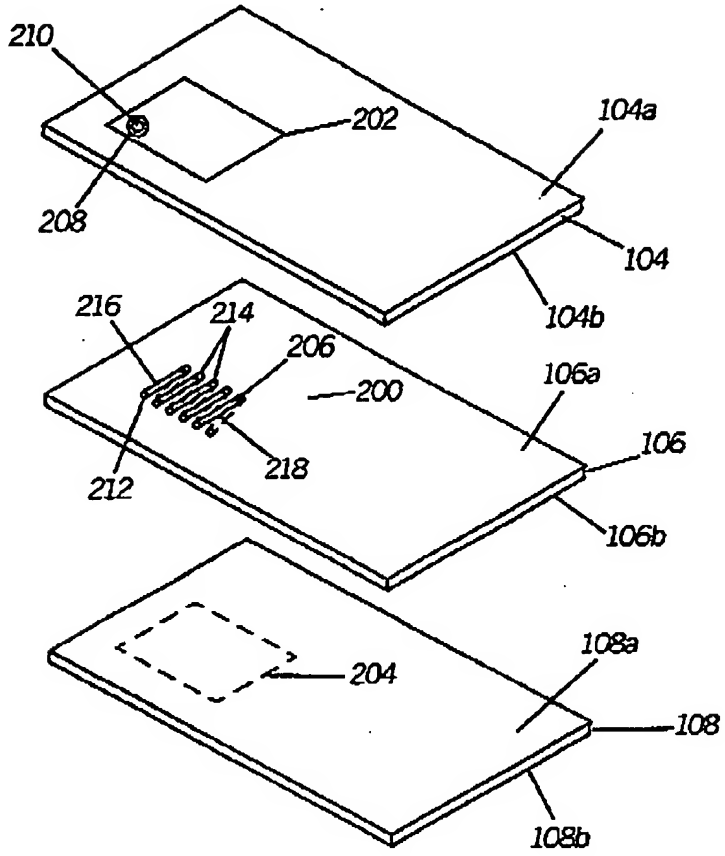
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FIG.6

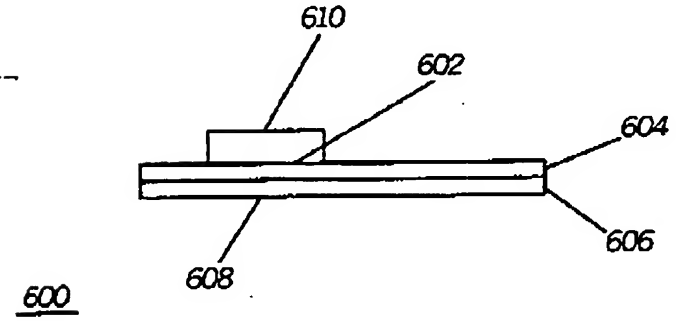
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FIG.5

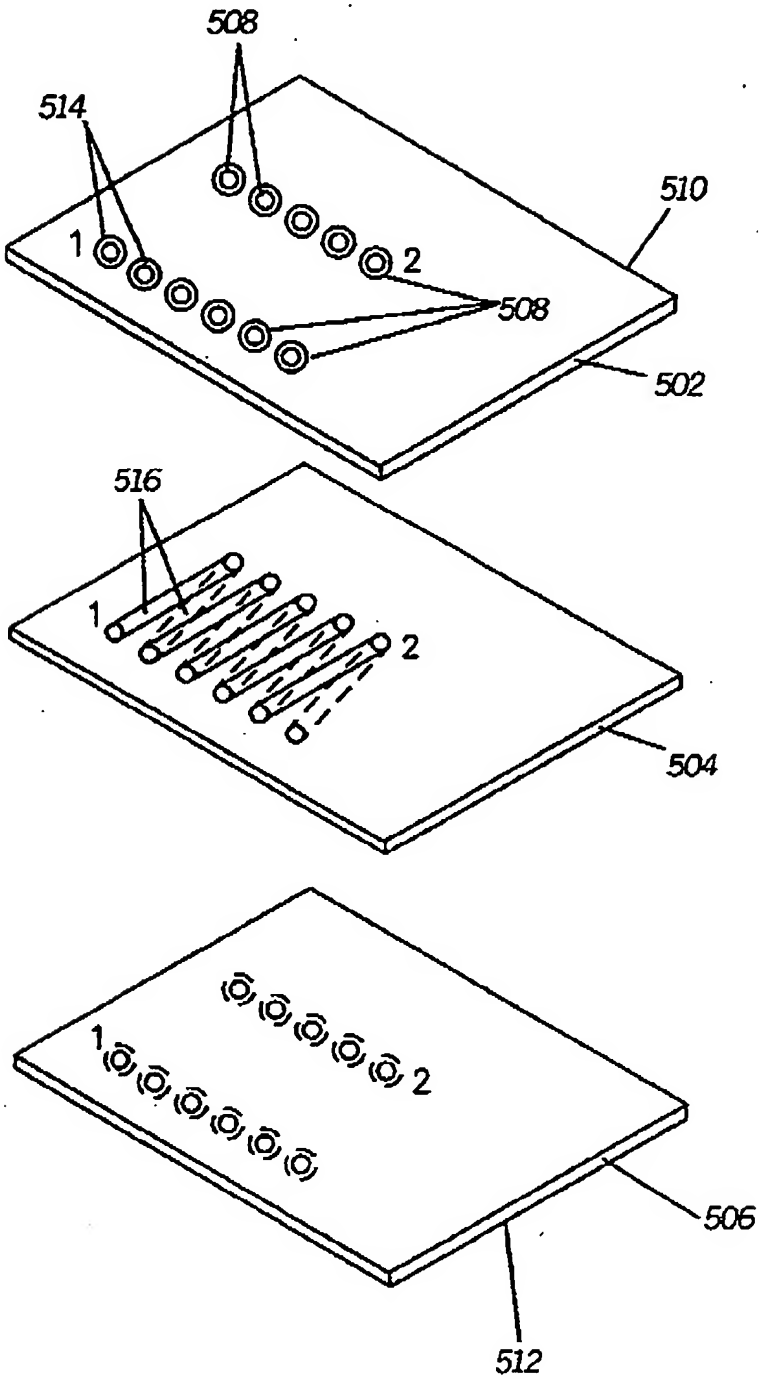


FIG. 7

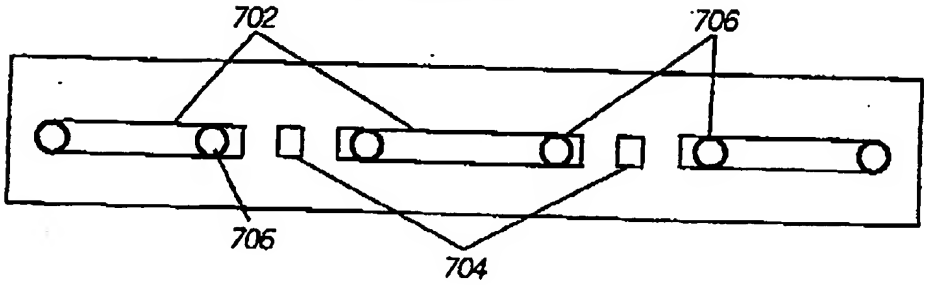


FIG. 8

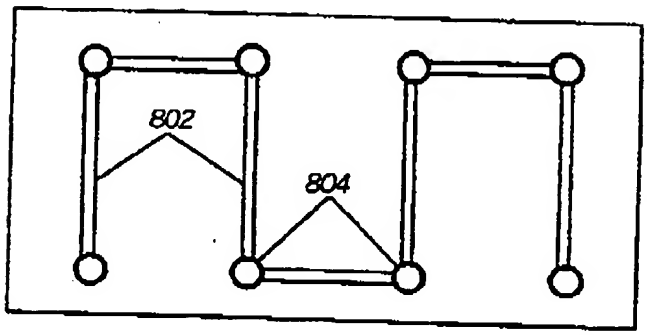
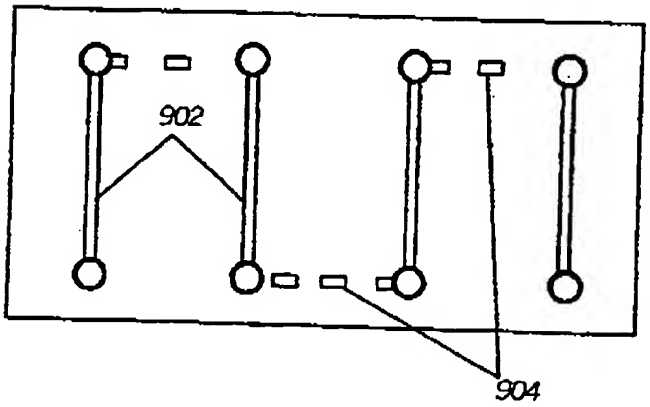


FIG. 9



PRINTED CIRCUIT BOARD INDUCTOR

TECHNICAL FIELD

This invention relates in general to electronic assemblies, and more specifically to an inductor formed on a printed circuit board.

BACKGROUND

Electronic circuit designers must constantly address the issue of interference such as radio frequency interference (RFI) and electromagnetic interference (EMI) which affect the performance of the circuits which they design. Typical solutions to interference problems include separating circuits from one another in order to minimize interference, placing metal "cans" over sensitive circuits or circuits which are the generators of interference signals (e.g., oscillator circuits, etc.). Another problem presented when designing electronic circuits such as radio circuits is minimizing the amount of board space required to implement a given circuit. Furthermore, in the case of some circuits such as filters and transmitter circuits, it is also important to design circuits which can be tuned or adjusted in order to overcome the changes in circuits due to component tolerance variations, etc.

Cost is also a consideration. An inductor which is built into the same printed circuit board as the rest of the circuitry reduces material does not add much additional cost to the manufacturing cost of the electronic assembly. Another issue confronted by designers is component tolerances. Inductor make tolerance is a factor which influences circuit design and sometimes leads to high cost, tight tolerance inductors. A printed circuit board inductor of the type described in the present invention can be constructed inexpensively into a printed circuit board, using dimensions and spacing that conform to the circuit board manufacturers process limitations and hold tighter make tolerances than their discrete counterparts. Furthermore, there is a need in the art for an inductor which can be tunable and which can provide for improved shielding against interference.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a side view of a multilayer circuit board in accordance with the invention.

FIG. 2 is an exploded view of some of the intermediate layers of the multilayer circuit board shown in FIG. 1.

FIG. 3 shows a tunable planar inductor having inductance adjustment means in accordance with the invention.

FIG. 4 shows a tunable planar inductor having an electronically adjustable inductance in accordance with the invention.

FIG. 5 shows an exploded view of similar intermediate layers as shown in FIG. 2, in this case using standard board construction techniques.

FIG. 6 shows another embodiment in which a printed circuit board inductor is shielded by a ground plane and a shield in accordance with the invention.

FIGS. 7–9 show different printed circuit board inductors in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

While the specification concludes with claims defining the features of the invention that are regarded as novel, it is believed that the invention will be better understood from a consideration of the following description in conjunction with the drawing figures.

Referring to FIG. 1, there is shown a populated multilayer printed circuit board 100 having a printed circuit board inductor in accordance with the present invention. Multilayer circuit board 100 as shown includes 6 layers 101, 102, 104, 106, 108 and 110. Preferably, the circuit board layers are formed from a glass reinforced epoxy such as FR4, or other materials used to form printed circuit boards. The top surface of multilayer circuit board 100 is populated with a plurality of electronic components 112 as is well known in the art. Although FIG. 1 is shown as a six layer multilayer board different number of layers can be designed for depending on the particular design requirements.

In FIG. 2, an exploded view of some of the intermediate layers 104, 106 and 108 of multilayer circuit board 100 are shown. In accordance with the invention, a printed circuit inductor 200 is formed on layer 106. Inductor 200 is formed by interconnecting metallization patterns 216 located on first surface 106a with metallization patterns 218 located on second surface 106B using interconnection vias 214. The vias could be blind or buried, as would be the case for a sequentially laminated circuit board, or the vias could penetrate each layer of the circuit board as will be discussed in reference to FIG. 5. Inductor 200 as shown forms a multiturn inductor having first 212 and second 206 terminals. In accordance with one embodiment of the present invention, the inductor 200 is shielded against external interference by ground planes 202 and 204 which are located so as to be in alignment or registration with inductor 200 when layers 104, 106 and 108 are mated together. When layers 101–110 are laminated together to form the multilayer board, ground planes 202 and 204 substantially overlay inductor 200, thereby providing interference protection to the inductor.

Ground plane 202 is formed by a metallization pattern located on first or top surface 104A of layer 104. Ground plane 204 is formed on the bottom or second surface 108B of layer 108. Metallization patterns 202 and 204 are electrically coupled to the multilayer circuit's ground potential using conventional runners (traces) and via interconnection techniques. In order to interconnect inductor 200 with other electronic components 112 located on multilayer board 100 one or both terminals 212 and 206 are interconnected to other layers of circuit board 100 using metallized vias. For example, terminal 212 can be electrically coupled to one of the upper layers 101 or 102 of circuit board 100 by providing a metallized via 210 in order to interconnect via 212 through layer 104 and up to a predetermined point on layer 101 or 102. In order to avoid short circuiting via 210 to ground plane 202, a non-metallized area 208 is provided between via 210 and ground plane 202. Preferably, the interconnection vias 210 used to interconnect the inductor 200 located in the intermediate layers of circuit board 100 are kept as short as possible in order to minimize effecting the inductance value of inductor 200 as well as prevent interference signals from effecting the circuit.

Although ground planes 202 and 204 reduce the inductance value of inductor 200 slightly, this change in inductance due to the shield can be compensated for by adjusting the dimensions of inductor 200. For example, the metallization runners 216, 218 can be decreased in width, the size of vias 214 can be decreased in size, more turn(s) can be added to the inductor, etc. Ground planes 202 although shown as not taking up the entire surface of the intermediate layers they reside on, could take substantially the entire surface of their corresponding layers if needed to improve shielding.

The overall area taken up to form inductor 200 is dictated

by the required inductance, the amount of current that the inductor will carry, the required Q (quality factor) of the inductor, and the minimum feature size available from the PCB vendor. A typical four turn coil would require an area of approximately 2.413 millimeter by 1.016 millimeter using conventional printed circuit manufacturing techniques, although smaller footprints can be achieved using more expensive printed circuit board manufacturing techniques.

In order to save manufacturing costs, instead of using blind vias as shown in FIG. 2 which cost more to manufacture, standard board construction can be used to manufacture the multilayer circuit board as shown in FIG. 5 in order to save costs. In FIG. 5, all the vias 508 shown go through all the layers of the multilayer circuit board including the intermediate layers 502, 504 and 506. In the case of ground plane layers 502 and 504, the vias are electrically isolated from the ground planes 510 and 512 by areas which surround each via 508 which are not plated. Ground plane 510 is located on the top surface of layer 502, while ground plane 512 is located on the bottom surface of layer 506 in order to isolate the ground planes from the traces 516.

Although the inductor 200 shown in FIG. 2 has been shown as an equivalent of air wound coil having the printed circuit board as the dielectric, other forms of printed circuit inductors can work with the present invention. Such as, inductors which are formed on one surface of the printed circuit board using no vias, other inductors which use two or more major surfaces of substrates to form, inductors which are straight lines or have other shapes, etc. In FIGS. 7-9 some other different printed circuit board inductors which can be used with the present invention are shown. FIG. 7 shows a straight line inductor having traces 702 on top surface and trace portions 704 on the bottom surface which are interconnected by vias 706. In FIG. 8, a single surface winding inductor which is formed by trace sections 802 which are interconnected by serial connecting vias 804 is shown. In FIG. 9, a dual surface inductor is shown having section 902 on the top surface and trace sections 904 on the bottom surface. Other types of inductor shapes and designs other than those shown can also be utilized.

When manufacturing electronic circuit boards, such as radio frequency circuits, it is sometimes required to tune the circuits during the manufacturing process. This is typically caused by component tolerance differences found between circuit boards due to variations between electronic components. In FIG. 3, a tunable printed circuit inductor 300 in accordance with another embodiment of the invention is shown. Inductor 300 includes a plurality of interconnection vias 306 which electrically interconnect top runners 308 with bottom runners 310. Inductor 300 includes two end terminals 302 and 304. In this embodiment, inductor 300 includes one or more inductance adjustment means which can take the form of metallized runners or trimmable resistors 316 and 318. Inductance adjustment runners 316 and 318 are metallized runners which short some of the turns of inductor 300. In order to increase the inductance value of inductor 300, one or more of the adjustment runners 316 are cut using well known laser trimming equipment or by simply mechanically cutting one or both runners 316, 318. Instead of metallized runners, laser trimmable resistors as known in the art having appropriate resistance values can be used, and trimmed in order to adjust the inductance value of inductor 200.

As shown in FIG. 3, with both inductance adjustment runners in place, inductor 300 forms a 2½ turn coil with its terminals being 302 and 312. If runner 316 is cut, the

inductor becomes a 3½ turn coil with its terminals being 302 and 314. Finally, if both of the inductance adjustment runners 316 and 318 are cut, the inductor becomes a 4½ turn coil, with terminals 302 and 304. Inductor 300 could be used for example, in a radio transmitter circuit wherein the power output of the transmitter could be adjusted during manufacture by trimming one or more of the inductance adjustment runners. If the vias 312, 314, and 304 where spaced appropriately, the runners 316 and 318 could be replaced with resistors, or zero ohm jumpers if desired, to decrease the inductance again.

FIG. 4 shows a tunable inductor or coil 400 having an electronically adjustable inductance value in accordance with the invention. Instead of using metallized runners 316 and 318 as shown in FIG. 3 in order to adjust the inductance value, in FIG. 4, a transistor 408 such as a field-effect transistor (FET), bipolar junction transistor (BJT) or other type of appropriate transistor as known in the art is used to automatically switch the inductance value of inductor 400. Transistor 408 is located between two adjacent turns of the printed circuit inductor 400. Transistor 408 is either in a first state where vias 406 and 404 are shorted together or in a second state where the transistor is open and there is no direct connection between vias 406 and 404. In the first state inductor 400 acts as a 3½ turn coil, while when transistor 408 is in the second state coil 400 acts as a 4½ turn coil.

Transistor 408 is switched from the first state to the second state by a control signal sent via line 410. The control signal can be generated by a number of conventional hardware circuits such as a microprocessor or other type of hardware circuit. Electronically tunable coil 400 provides the ability of adjusting the inductance value of inductor 400 even when inductor 400 is formed within intermediate layers of a multilayer circuit board as shown in FIG. 1. This provides the opportunity of having an inductor located within a multilayer circuit board as discussed with reference to FIG. 1 and still be able to adjust its inductance value. Electronically tunable inductor 400 can be used for many electronic circuits where a tunable inductor is required. For example, in radio transmitter circuits in order to adjust the power output level, etc.

In FIG. 6, another embodiment of the present invention in which a printed circuit board inductor 602 is shielded by a ground plane 608 and a shield 610 is shown. In this embodiment, a printed circuit board inductor is formed on substrate 604 similar to that shown in FIG. 2. A second substrate 606 having a ground plane 608 etched on the bottom layer is attached to the first substrate 604. And a shield such as a metal can 610 is attached to the top layer of substrate 604 in order to fully shield inductor 602 from interference. Inductor 602 can include the inductance tuning means previously discussed if tuning is a requirement.

In summary, the present invention provides for a shielded planar inductor which can be used in environments were a shielded inductor is required, such as in radio frequency circuit applications. By locating the inductor within the intermediate layers of a multi-layer circuit board, board space on the top surface of the multi-layer circuit board is conserved for other electronic components. In another aspect of the present invention, a planar printed circuit board inductor 300 or 400 includes an inductance tuning means such as metallized runners 316, 318, an electronic switching device 408, or other means in order to adjust the inductance value. The electronically tunable inductor shown in FIG. 4 can also be formed within intermediate layers of a multilayer circuit board in order to conserve board space and also to allow the inductor to be shielded if required.

What is claimed is:

1. An electronic assembly, comprising:

a multilayer circuit board including first and second substrate layers each having first and second major surfaces;

an inductor formed on the second substrate layer;

a first ground plane located on the first major surface of the first substrate layer;

the second major surface of the first substrate layer is attached to the first major surface of the second substrate layer such that the first ground plane is located in substantial registration with the inductor;

an electronic switch operable between first and second states and coupled between two of the metallization vias such that the inductor has a first inductance value when the electronic switch is in the first state and a second inductance value when the electronic switch is in the second state; and

wherein the second substrate layer has first and second major surfaces and the inductor includes a series of metallization runners on the first and second major surfaces which are serial interconnected with each other through the second intermediate layer by a plurality of metallized vias.

2. An electronic assembly as defined in claim 1, further comprising a third intermediate substrate layer having first and second major surfaces;

a second ground plane located on the second major surface of the third substrate layer; and

the first major surface of the third substrate layer is attached to the second major surface of the second substrate layer and the second ground plane is in substantial registration with the first ground plane and the inductor.

3. An electronic assembly as defined in claim 1, wherein substrate layers are formed from glass reinforced epoxy.

4. An electronic assembly as defined in claim 1, further comprising a runner electrically coupling two of the metallization vias together such that at least one of the serially connected metallization runners is electrically bypassed so as to lower the inductance value of the inductor.

5. An assembly, comprising:

a first substrate;

an inductor formed on the first substrate, the inductor including a series of metallization runners which are serial interconnected with each other by a plurality of metallized vias; and

an inductance adjustment means coupled between two of said plurality of metallized vias, wherein the inductance adjustment means comprises a transistor which can switch between first and second states, and when in the first state the inductance value of the inductor is a first value and when in the second state the inductance value of the inductor is a second value.

6. An assembly as defined in claim 5, wherein the inductance adjustment means comprises a metallized runner.

7. An assembly as defined in claim 5, wherein the inductance adjustment means comprises a trimmable resistor.

8. An assembly as defined in claim 5, further comprising:

a second substrate;

a ground plane located on the second substrate; and

the first and second substrate are attached to each other.

9. An assembly as defined in claim 8, wherein the ground plane substantially overlays the inductor.

10. A multilayer printed circuit board assembly comprising:

a first printed circuit board layer having an inductor formed on the printed circuit board layer;

a second printed circuit board layer attached to the first printed circuit board layer having a ground plane which substantially overlays the inductor; and

an electronic switch operable between first and second states and such that the inductor has a first inductance value when the electronic switch is in the first state and a second inductance value when the electronic switch is in the second state.

11. A multilayer printed circuit board assembly as defined in claim 10, further comprising:

a shield attached to the first printed circuit board layer such that the shield and ground plane sandwich the inductor between them.

* * * * *

US006459352B1

(12) **United States Patent**
Liu et al.

(10) **Patent No.: US 6,459,352 B1**
(45) **Date of Patent: Oct. 1, 2002**

(54) **ON-CHIP TRANSFORMERS**

(75) Inventors: **Q. Z. Liu**, Irvine, CA (US); **David Howard**, Irvine, CA (US)

(73) Assignee: **Skyworks Solutions, Inc.**, Newport Beach, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 18 days.

(21) Appl. No.: 09/779,402

(22) Filed: Feb. 8, 2001

(51) Int. Cl.[7] H01F 5/00

(52) U.S. Cl. 336/200; 336/223; 336/232

(58) Field of Search 336/200, 223, 336/232; 29/602.1

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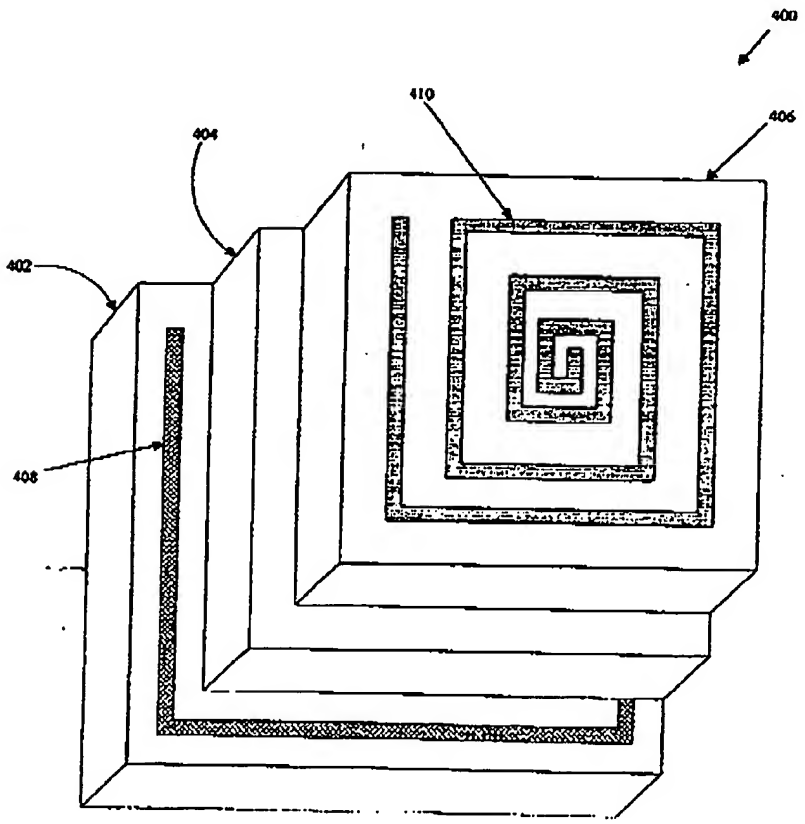
Primary Examiner—Anh Mai
(74) *Attorney, Agent, or Firm*—Farjami & Farjami LLP

(57) **ABSTRACT**

In an exemplary embodiment of the disclosed transformer, the transformer comprises a dielectric area. For example, the dielectric area can consist of three different dielectric layers. Also, by way of example, the dielectric area can comprise silicon dioxide or a low-k dielectric. According to the exemplary embodiment, the dielectric area is interspersed with a permeability conversion material. The permeability conversion material has a permeability higher than the permeability of the dielectric area. For example, the permeability conversion material can be nickel, iron, nickel-iron alloy, or magnetic oxide. The exemplary embodiment further comprises a first conductor and also a second conductor patterned into the dielectric area. The first and/or the second conductor can comprise copper, aluminum, or a copper-aluminum alloy. Each of the first and second conductors are made up of a number of turns which result in, respectively, the primary and secondary windings of the exemplary disclosed transformer.

19 Claims, 5 Drawing Sheets



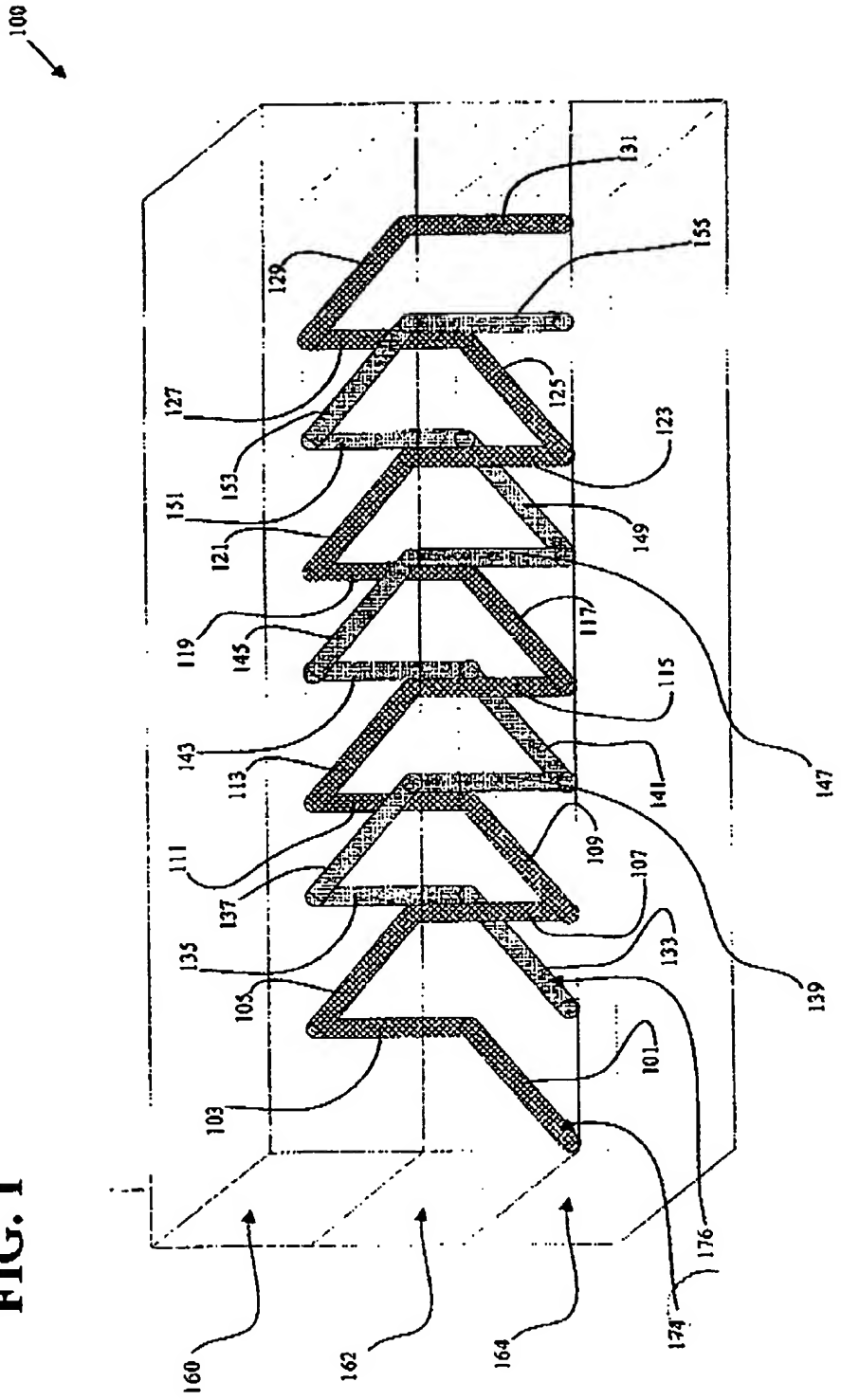

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FIG. 1

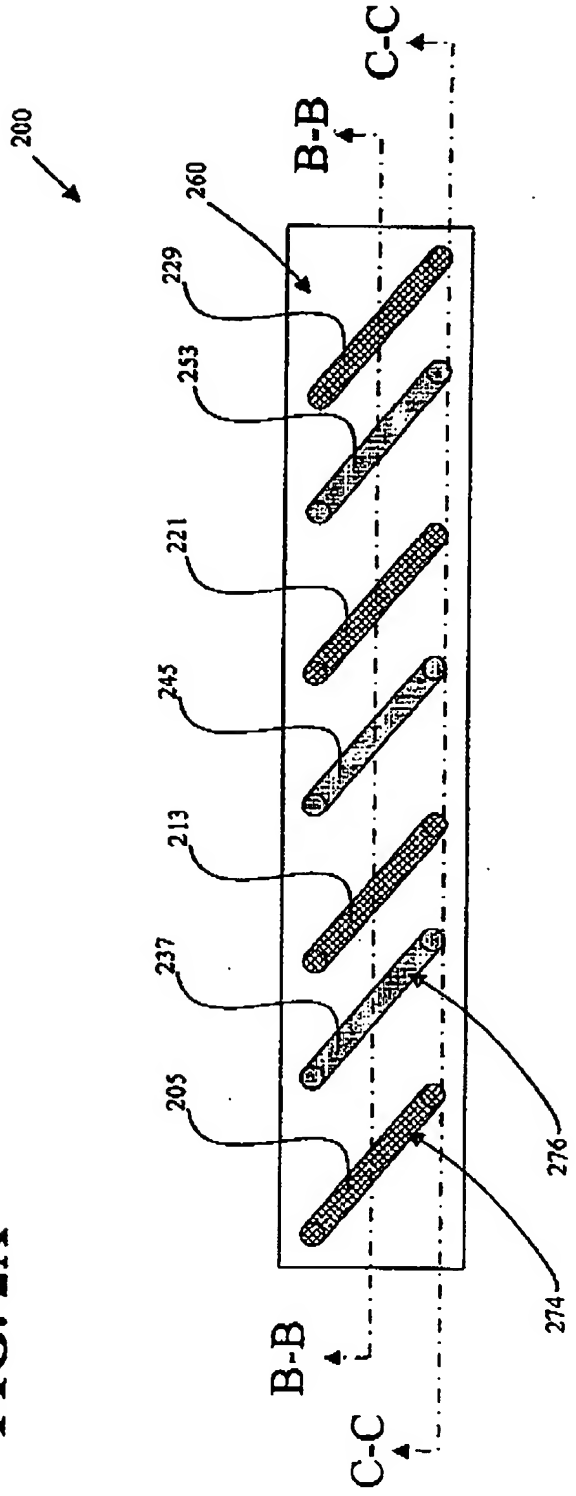

FIG. 2A

FIG. 2B

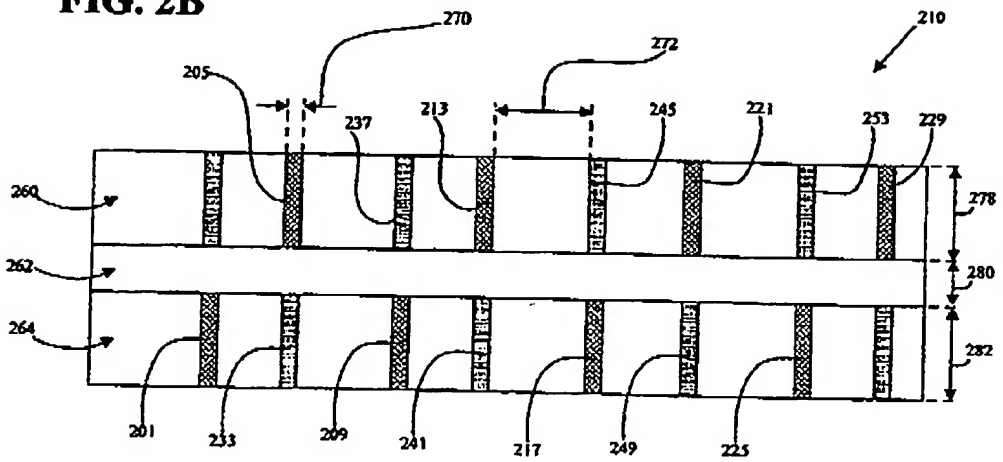
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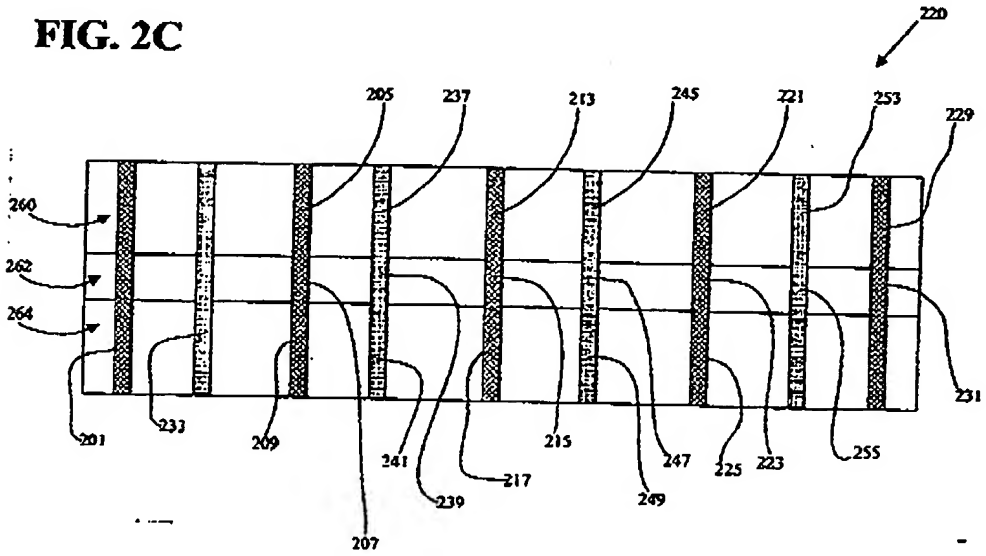
FIG. 2C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262
264
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FIG. 3

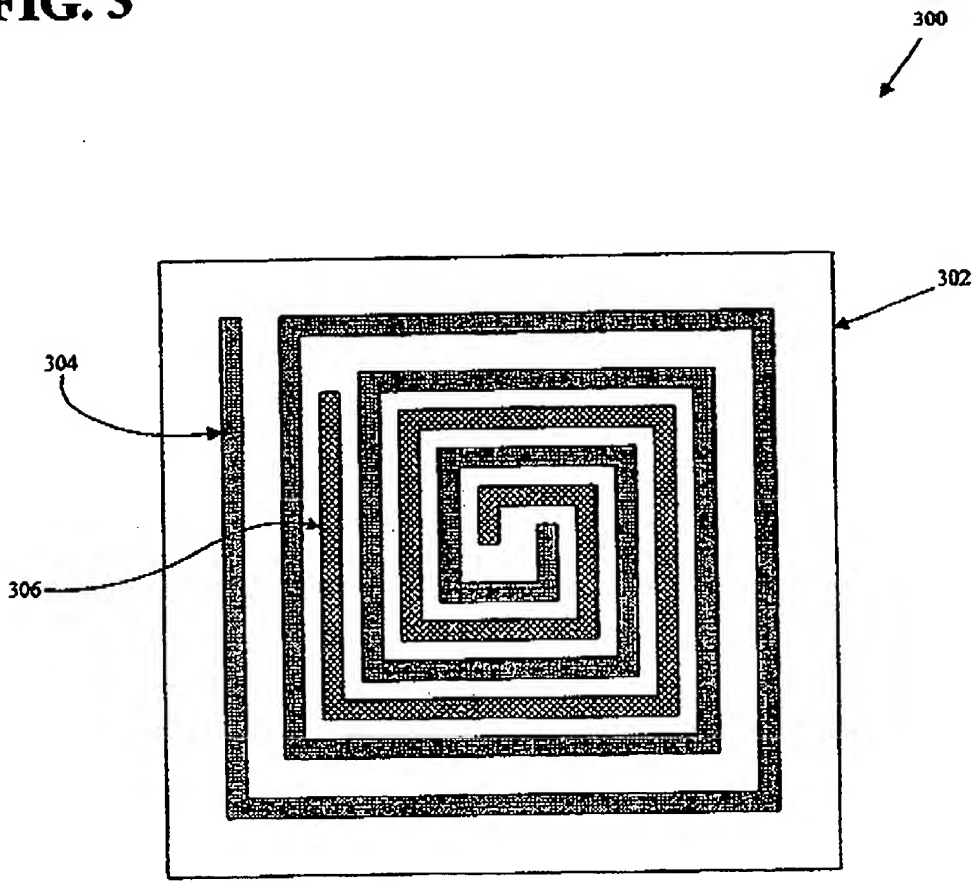
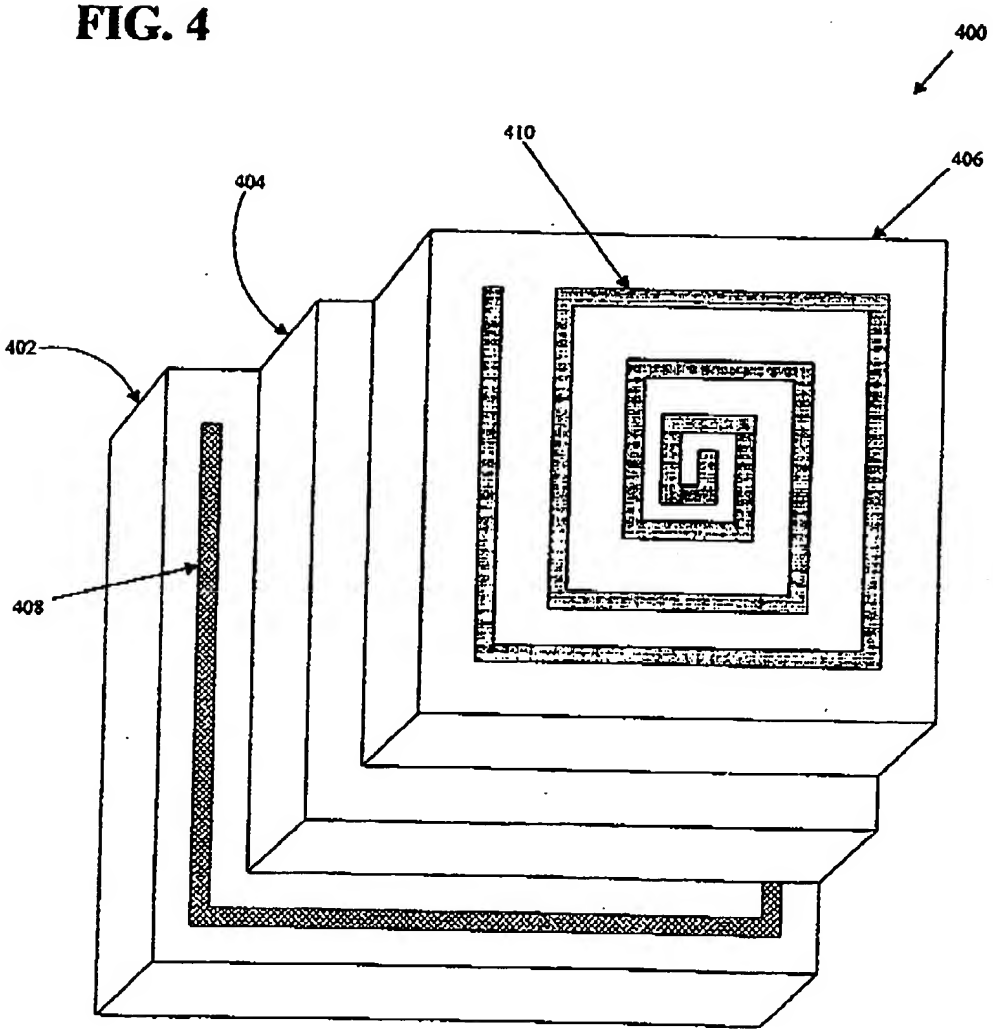


FIG. 4



ON-CHIP TRANSFORMERS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is generally in the field of fabrication of electronic circuit components. In particular, the present invention is in the field of fabrication of transformers used in electronic circuits.

2. Background Art

It is known in the art that there is an ever-present demand for decreasing electronic circuit component sizes and geometries. The demand is fueled, in large part, by the consumers' desire for ever-smaller communication and information processing devices, such as cellular telephones, laptop computers, and hand-held information assistants. The requirement to decrease the size of these consumer communication and information processing devices has resulted, among other things, in a need to reduce the size of the electronic components these devices contain. As a result, semiconductor device sizes and geometries have decreased dramatically, with each unit area of the semiconductor die supplying greater computing power and functionality. This has resulted in Ultra Large Scale Integration (ULSI) chips containing over a million components per chip. However, the transformer, an off-chip electronic component, has not benefited from this dramatic decrease in size.

The discrete, off-chip transformer suffers from various disadvantages not shared by on-chip electronic components. The off-chip transformer eventually goes through a wire bond for connection to on-chip circuitry. The off-chip transformer also requires assembly of at least two components (i.e. the chip itself and the off-chip transformer). The required assembly of two or more components introduces corresponding reliability issues and also results in a greater manufacturing cost.

By way of background, a transformer is comprised essentially of two cross-coupled inductors. The magnetic coupling between the two inductors is called mutual inductance. Discrete inductors are typically coils wound around a common core. The quality factor ("Q") of an inductor is determined by Q=L/R, where L is the inductance and R is the resistance inherent in the inductor. A relatively low quality factor signifies a relatively high energy loss. Since it is desirable to have a large quality factor in an inductor, it is desirable to have a large quality factor in each of the transformer's separate inductors. This can be accomplished by either increasing the inductance of the inductors, or decreasing their respective resistances.

The problems encountered when attempting to increase inductance or reduce resistance can be illustrated by using the example of an on-chip square spiral inductor. Such an inductor is disclosed in a co-pending United States patent application entitled "Method for Fabrication of On-Chip Inductors and Related Structure," Ser. No. 09/627,505 filed Jul. 28, 2000, and assigned to the assignee of the present application. The disclosure in that co-pending application is hereby incorporated fully by reference into the present application. As discussed in that co-pending application, the inductance of a conventional on-chip square spiral inductor can be increased by increasing the spiral diameter of the on-chip inductor. However, such an increase would make the conventional on-chip inductor even larger and would require even more chip space. For example, typical inductor values for a square spiral inductor used in mixed signal circuits and in RF applications range from 1 to 100 nano-henrys. If a

circuit in a semiconductor chip required a square spiral inductor with a value of 30 nano-henrys and a fabrication process with a metal pitch of 5.0 microns is used, the inductor would require 17 metal turns and would have a spiral diameter of approximately 217 microns. As such, even a 30 nano-henry conventional on-chip inductor would require a considerable amount of chip space.

For the square spiral on-chip inductor in our example, for a given spiral diameter, the inductance is proportional to n^2, where n is the number of metal turns. Therefore, the inductance can be increased by increasing the number of turns. However, as the number of metal turns increases, the overall resistance of the metal turns will also increase. The increase in the overall resistance of the inductor will decrease the quality factor of the inductor. Thus, if the on-chip inductor in our example were coupled with another similar on-chip inductor to create a transformer, there would be a significant energy loss in the transformer.

Turning attention again to off-chip transformers, a discrete (i.e. off-chip) transformer also requires relatively long off-chip wires and interconnect lines to connect the transformer terminals to on-chip devices. The relatively long off-chip wires and interconnect lines result in added and unwanted resistance, capacitance, and inductance. Energy would be lost due to this unwanted resistance, capacitance, and inductance. Additionally, the interconnects for off-chip transformers are subject to long-term damage from vibration, corrosion, chemical contamination, oxidation, and other chemical and physical forces. Exposure to vibration, corrosion, chemical contamination, oxidation, and other chemical and physical forces results in lower long-term reliability for off-chip transformers.

Surface-mount packages that integrate both isolation transformers and common mode chokes utilizing the same footprint as discrete transformer-only products have been used to optimize board layout by allowing more functionality in the same amount of space. This approach has been necessitated by the ever higher density requirements of telephony and networking devices such as ISPs, multiplexers, wide area networks (WANS), internetworking interfaces, digital access and cross connect systems (DACS), channel banks and cellular base stations. Although this is an important step in meeting the need for reduced-size transformers, these modules are still discrete devices. They still require board assembly, with its attendant manufacturing cost and reliability issues.

Planar-transformer technology is another attempt at reducing transformer size. In this technology, multiple layers of a multilayer printed circuit board ("PCB") are sandwiched together to form the transformer windings. The core is formed in two sections that reside on the top and bottom of sandwiched windings. This technology reduces the transformer size and provides adequate unit-to-unit repeatability. However, as with surface-mount packages, planar-transformers are discrete devices that still require board assembly.

To applicants' knowledge, there are no known attempts to fabricate on-chip transformers. However, even if such an attempt were made, it would be very difficult to place a transformer inside the semiconductor die using presently known techniques. Some of the reasons for this difficulty include the following. First, fabricating each of the required on-chip inductors with high inductance values for use as a transformer winding is difficult because the size of the inductor is too large for the semiconductor die. Some of the reasons for the large size of conventional on-chip inductors

were discussed above. Thus, the individual inductor's size limits the use of on-chip inductors to build on-chip transformers for RF and mixed signal circuits. Second, the inductor's quality factor would be too low. As explained above, when a higher inductance is desired and is achieved by increasing the number of metal turns, i.e. the windings, of the inductor, the corresponding increase in the resistance of the inductor results in a lower quality factor.

Thus, there is a need in the art for a transformer that has a small size, high quality factor inductor windings, is reliable, cost-effective, and which does not require connections through off-chip wires or off-chip interconnect lines.

SUMMARY OF THE INVENTION

The present invention is directed to on-chip transformers. The present invention discloses a transformer which has a small size, high quality factor inductor windings, is reliable, cost-effective, and which does not require connections through off-chip wires or off-chip interconnect lines.

In an exemplary embodiment of the invention's transformer, the transformer comprises a dielectric area. For example, the dielectric area can consist of three different dielectric layers. Also, by way of example, the dielectric area can comprise silicon dioxide or a low-k dielectric. According to the exemplary embodiment, the dielectric area is interspersed with a permeability conversion material. The permeability conversion material has a permeability higher than the permeability of the dielectric area. For example, the permeability conversion material can be nickel, iron, nickel-iron alloy, or magnetic oxide.

The exemplary embodiment of the invention's transformer further comprises a first conductor and also a second conductor patterned into the dielectric area. The first and/or the second conductor can comprise, for example, copper, aluminum, or a copper-aluminum alloy. Each of the first and second conductors are made up of a number of turns which result in, respectively, the primary and secondary windings of the exemplary embodiment of the invention's transformer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a perspective view of an embodiment of the invention's transformer.

FIG. 2A illustrates a top view of the embodiment of the invention's transformer shown in FIG. 1.

FIG. 2B illustrates a cross-sectional view along the line B—B in FIG. 2A of the embodiment of the invention's transformer shown in FIG. 1.

FIG. 2C illustrates a cross-sectional view along the line C—C in FIG. 2A of the embodiment of the invention's transformer shown in FIG. 1.

FIG. 3 illustrates a top view of another embodiment of the invention's transformer.

FIG. 4 illustrates a perspective view of yet another embodiment of the invention's transformer.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to on-chip transformers. The following description contains specific information pertaining to different types of materials, layouts, dimensions, and implementations of the invention's transformer. One skilled in the art will recognize that the present invention may be practiced with material, layout, or dimensions, different from those specifically discussed in the present application. Moreover, some of the specific details of the invention are not discussed in order not to obscure the invention. The specific details not described in the present application are within the knowledge of a person of ordinary skills in the art.

The drawings in the present application and their accompanying detailed description are directed to merely example embodiments of the invention. To maintain brevity, other embodiments of the invention that use the principles of the present invention are not specifically described in the present application and are not specifically illustrated by the present drawings.

FIG. 1 shows perspective view 100 of an exemplary embodiment of the invention's transformer. The present embodiment's transformer, whose perspective view 100 is shown in FIG. 1, is used for illustration purposes only. In other words, FIG. 1 does not depict the relative sizes of various elements, and does not show the relative thicknesses and depths of various elements and is not drawn to scale. Also, FIG. 1 shows only a section of the invention's transformer. FIG. 2A shows a top view 200 of the invention's transformer corresponding to perspective view 100 of the same transformer shown in FIG. 1. FIG. 2B shows cross-sectional view 210 along line B—B of FIG. 2A of the same transformer while FIG. 2C shows cross-sectional view 220 along line C—C of FIG. 2A of that same transformer. As such, FIGS. 1, 2A, 2B, and 2C depict various views of the same exemplary embodiment of the invention's transformer.

In FIG. 1, the primary winding of the invention's transformer, also called a "first conductor" in the present application, is referred to generally by numeral 174. In the present example, primary winding 174 consists of a number of "turns" made up of segments 101, 103, 105, 107, 109, 111, 113, 115, 117, 119, 121, 123, 125, 127, 129, and 131. The secondary winding of the invention's transformer, also called a "second conductor" in the present application, is referred to generally by numeral 176. In the present example, secondary winding 176 consists of a number of "turns" made up of segments 133, 135, 137, 139, 141, 143, 145, 147, 149, 151, 153, and 155.

The primary winding 174 segments 101, 103, 105, 107, 109, 111, 113, 115, 117, 119, 121, 123, 125, 127, 129, and 131 can be grouped into via metal segments 103, 107, 111, 115, 119, 123, 127, and 131, and interconnect metal segments 101, 105, 109, 113, 117, 121, 125, and 129. Likewise, the secondary winding 176 segments 133, 135, 137, 139, 141, 143, 145, 147, 149, 151, 153, and 155 can be grouped into via metal segments 135, 139, 143, 147, 151, and 155, and interconnect metal segments 133, 137, 141, 145, 149, and 153.

As stated above, FIG. 2A represents top view 200 of the invention's transformer whose perspective view 100 was shown in FIG. 1. As such, dielectric layer 260 in FIG. 2A corresponds to dielectric layer 160 in FIG. 1. As stated above, FIGS. 2B and 2C show two different cross-sectional views 210 and 220 corresponding to perspective view 100 of the invention's transformer shown in FIG. 1. As seen in FIG. 2A, cross-sectional view 210 in FIG. 2B is taken along line B—B which is deep inside the invention's transformer. Further, as seen in FIG. 2A, cross-sectional view 220 in FIG. 2C is taken along line C—C that is at the outside edge of the invention's transformer. Dielectric layer 260 in FIG. 2B and dielectric layer 260 in FIG. 2C correspond to dielectric layer 260 in FIG. 2A and also to dielectric layer 160 in FIG. 1. Dielectric layer 262 in FIG. 2B and dielectric layer 262 in

FIG. 2C correspond to dielectric layer 162 in FIG. 1. Dielectric layer 264 in FIG. 2B and dielectric layer 264 in FIG. 2C correspond to dielectric layer 164 in FIG. 1. Dielectric layers 260, 262, and 264 are also collectively referred to as a "dielectric area" in the present patent application.

Also, in the present embodiments of the invention as well as in other embodiments not discussed herein, there can be a dielectric layer below dielectric layer 264 and/or a dielectric layer above dielectric layer 260. Dielectric layers which can exist below dielectric layer 264 and above dielectric layer 260 are not shown in the drawings of the present application to preserve simplicity. Nevertheless, the existence and methods for fabrication of such additional dielectric layers are known to a person of ordinary skill in the art.

Interconnect metal segments 205, 213, 221, and 229 of primary winding 274 shown in FIGS. 2A, 2B, and 2C correspond respectively to interconnect metal segments 105, 113, 121, and 129 of primary winding 174 shown in FIG. 1. Likewise, interconnect metal segments 237, 245, and 253 of secondary winding 276 in FIGS. 2A, 2B, and 2C correspond respectively to interconnect metal segments 137, 145, and 153 of secondary winding 176.

Interconnect metal segments 205, 213, 221, 229, 237, 245, and 253 in FIGS. 2B and 2C are shown extending through dielectric layer 260, whereas corresponding interconnect metal segments 105, 113, 121, 129, 137, 145, and 153 in FIG. 1 are shown only on the bottom plane of dielectric layer 160.

Interconnect metal segments 201, 209, 217, and 225 of primary winding 274 in FIGS. 2B and 2C, correspond to interconnect metal segments 101, 109, 117, and 125 of primary winding 174 in FIG. 1. Also, interconnect metal segments 233, 241, and 249 of secondary winding 276 in FIGS. 2B and 2C correspond to interconnect metal segments 133, 141, and 149 of secondary winding 176 in FIG. 1.

Via metal segments 207, 215, 223, and 231 of primary winding 274 in FIG. 2C correspond to via metal segments 107, 115, 123, and 131 of primary winding 174 in FIG. 1. Via metal segments 239, 247, and 255 of secondary winding 276 in FIG. 2C correspond to via metal segments 139, 147, and 155 of secondary winding 176 in FIG. 1. Via metal segments 207, 215, 223, and 231 of prim ary winding 274 in FIG. 2C and via metal segments 239, 247, and 255 of secondary winding 276 in FIG. 2C are not shown in FIG. 2B because cross-sectional view 210 in FIG. 2B is taken along line B—B which is deep inside the invention's transformer, whereas cross-sectional view 220 in FIG. 2C is taken along line C—C which is at the outside edge of the invention's transformer.

As shown in FIG. 2B, the separation between each interconnect metal segment of primary winding 274 and an immediately adjacent interconnect metal segment of secondary winding 276 is indicated by numeral 272. In the present embodiment of the invention, separation 272 is between approximately 0.25 and approximately 10 microns. However, separation 272 may vary without departing from the scope of the present invention. As shown in FIG. 2B, the width of the interconnect metal segments in primary winding 274 and the width of interconnect metal segments in secondary winding 276 is referred to by numeral 270 in FIG. 2B. In the present embodiment of the invention, width 270 is between approximately 0.25 and 10 microns. However, width 270 may vary without departing from the scope of the present invention.

As shown in FIG. 2B, the thickness of dielectric layer 260 is referred to by numeral 278. Further, as shown in FIG. 2B, the thickness of dielectric layer 264 is referred to by numeral 282. In the present embodiment of the invention, thickness 278 of dielectric layer 260 is between approximately 1,000 and 30,000 Angstroms while thickness 282 of dielectric layer 264 is also between approximately 1,000 and 30,000 Angstroms. However, thicknesses 278 and 282 may vary without departing from the scope of the present invention. As further shown in FIG. 2B, the thickness of dielectric layer 262 is referred to by numeral 280 in FIG. 2B. In the present embodiment of the invention, thickness 280 of dielectric layer 262 is between approximately 1,000 and 6,000 Angstroms. However, thickness 280 may vary without departing from the scope of the present invention.

In two alternative embodiments of the present invention, interconnect metal segments, such as interconnect metal segments 105 and 137 in the primary and secondary windings (FIG. 1), may be patterned within dielectric layer 160 (FIG. 1) by either a damascene process or by a subtractive etching process. Similarly, interconnect metal segments, such as interconnect metal segments 109 and 133 in the primary and secondary windings, may be patterned within dielectric layer 164 by either a damascene process or by a subtractive etching process. In the damascene process, trenches are cut into the dielectric and then filled with metal. Then excess metal over the wafer surface is removed by a chemical mechanical polish process ("CMP") to form desired interconnect metal patterns within the trenches. Generally copper is used in a damascene process; however, other metals such as aluminum can also be used. In the subtractive etching process, a blanket layer of metal is uniformly deposited on a given surface. Thereafter, through masking and etching steps, a desired pattern is formed by etching away the unwanted portions of the blanket layer of metal. As such, what remains is a desired pattern of interconnect metal. Generally aluminum or aluminum-copper alloys are used in a subtractive etching process; however, other metals can also be used.

Via metal segments, such as via metal segments 103 and 107 in the primary winding 174 in FIG. 1 and via metal segments 135 and 139 in the secondary winding 176 in FIG. 1, may be fabricated in a damascene process using copper or tungsten and in a subtractive etching process using tungsten in a manner known in the art. Moreover, in a damascene process, via metal segments may be fabricated by using either a "via first" or a "trench first" process, which are both known in the art. Generally, the dielectric material that comprises dielectric layers 260, 262 and 264 (FIGS. 2B and 2C) can be silicon dioxide, or a low-k dielectric such as porous silica, fluorinated amorphous carbon, fluoropolymer, parytene, polyarylene ether, silsesquioxane, fluorinated silicon dioxide, and diamondlike carbon.

By way of background, when a material is placed within the magnetic field of an inductor, the magnetic dipoles of the material interact with the magnetic field created by the inductor. If the magnetic filed of the inductor is reinforced by the magnetic moments, a larger number of flux lines are created, thus increasing the inductance. There are essentially two cross-coupled inductors in a transformer. The inductance caused by flux coupling between the two inductors is called the mutual inductance. The mutual inductance is equal to the coupling coefficient of the two coils multiplied by the square root of the product of the inductance of each coil.

If the magnetic fields of the cross-coupled inductors are reinforced by the magnetic moments, a larger number of flux lines are created, thus increasing the mutual inductance of the transformer. The ability of a material to reinforce the

magnetic fields of the cross-coupled inductors is determined by the permeability of the material. Permeability is the property of a material that describes the magnetization developed in that material when excited by a magnetic field. For an inductor, as is well known in the art, the magnitude of inductance is proportional to permeability of the materials that surround the inductor.

The mutual inductance of the present embodiment of the invention's transformer may be increased by increasing the permeability in any of dielectric layers 160, 162, or 164 in FIG. 1 (corresponding to dielectric layers 260, 262, and 264 in FIGS. 2B and 2C) or in a combination of any two of the dielectric layers or in all three of the dielectric layers.

One method that may be used in the present invention to increase permeability of dielectric layers 160, 162, and/or 164 is by introducing into the dielectric layer (or dielectric layers) atoms and/or molecules of high permeability materials. These high permeability atoms and/or molecules will increase the permeability of the dielectric layer significantly. The high permeability atoms and/or molecules can be introduced into the dielectric layer using ion implantation or ion sputtering techniques.

As an example, ion implantation can be used to introduce ions of high permeability materials into dielectric layers 160, 162, or 164 of the invention's transformer. More specifically, a high current ion implanter could be used to ionize and separate individual atoms of the high permeability material, such as iron or nickel, accelerate and form them into a beam which would be swept across the surface of the dielectric layer. The individual ions would penetrate the surface of the dielectric layer and come to a stop below the surface of the dielectric layer. It is noted that in the present application the term "ions" is used generally to refer to ionized atoms, ionized clusters of atoms, or ionized molecules. Also, the ion implanter used to implant ions in the dielectric layer is used in many other ion implantation steps required for fabricating semiconductor chips, such as to implant arsenic, boron, and argon ions into the chip to form doped regions on the chip.

As an example, iron ions could be implanted in any of the dielectric layers 160, 162, or 164 of the present invention's transformer to increase permeability. In the alternative, nickel ions or ions from other high permeability metals could be implanted. Further, a metal alloy can be implanted in dielectric layers 160, 162, or 164 of the invention's transformer by implanting ions of different metals in doses that correspond to the ratio of the different atoms in the alloy and in energies that give matched implantation depth profile. The different ions of the alloy can be implanted during separate implantation steps. This metal alloy implantation may be desirable, as some metal alloys have higher permeability than the individual metals alone. The above described technique for increasing dielectric permeability by implantation or sputtering of high permeability ions is disclosed in a co-pending United States patent application entitled "Method for Fabrication of On-Chip Inductors and Related Structure," Ser. No. 09/627,505 filed Jul. 28, 2000, and assigned to the assignee of the present application. The disclosure in that co-pending application is hereby incorporated fully by reference into the present application.

Other methods exist for increasing the permeability of the dielectric layer or layers through which the magnetic field flux lines traverse. For example, trenches can be etched into the dielectric regions next to the interconnect metal segments of the primary winding or the secondary winding of the transformer. The trenches are then filled with a material having a permeability substantially higher than the permeability of the dielectric. The high permeability material can be, for example, nickel, iron, nickel-iron alloy, or magnetic oxide. As a result, the inductance values of the primary and/or secondary windings of the transformer are significantly increased. This method for increasing dielectric permeability is disclosed in a co-pending United States patent application entitled "Method for Fabrication of High Inductance Inductors and Related Structure," Ser. No. 09/649,442 filed Aug. 25, 2000, and assigned to the assignee of the present application. The disclosure in that co-pending application is hereby incorporated fully by reference into the present application.

Another method for increasing the permeability of the pertinent dielectric layer or layers is to deposit a spin-on matrix containing high permeability particles in the pertinent dielectric layer or layers and immediately next to, below, or above, the interconnect metal segments that make up the primary winding or the secondary winding of the transformer. For example, the high permeability spin-on matrix can be deposited between interconnect metal segments forming the primary winding or the secondary winding of the transformer. The high permeability particles can comprise, for example, nickel, iron, nickel-iron alloy, or magnetic oxide. As a result, the inductance values of the primary and/or secondary windings of the transformer are significantly increased. This method for increasing dielectric permeability is disclosed in a co-pending United States patent application entitled "Method for Fabricating On-Chip Inductors and Related Structure," Ser. No. 09/658,483 filed Sep. 8, 2000, and assigned to the assignee of the present application. The disclosure in that co-pending application is hereby incorporated fully by reference into the present application.

Yet another method for increasing the permeability of the pertinent dielectric layer or layers is to deposit a blanket layer of high permeability material over the pertinent dielectric layer or layers. The high permeability layer can comprise, for example, nickel, iron, nickel-iron alloy, or magnetic oxide. The blanket deposition of the layer of high permeability material can be accomplished by, for example, a sputtering technique. After depositing the high permeability layer, a portion of the atoms or molecules in the high permeability material is driven into the underlying dielectric which surrounds the interconnect metal segments of the primary winding or the secondary winding of the invention's transformer. As a result, the permeability of the underlying dielectric and the inductance values of the primary and/or secondary windings of the transformer are significantly increased. This method for increasing dielectric permeability is disclosed in a co-pending United States patent application entitled "Method for Increasing Inductance of On-Chip Inductors and Related Structure," U.S. Ser. No. 09/668,790 filed Sep. 22, 2000, and assigned to the assignee of the present application. The disclosure in that co-pending application is hereby incorporated fully by reference into the present application.

The implantation, sputtering, or any of the other methods described above, used to introduce high permeability material into the dielectric material which surrounds an inductor is collectively referred to as "interspersing" in the present application. The high permeability material that is interspersed into the dielectric material is also referred to as a "permeability conversion material." Examples of permeability conversion material that are interspersed into the dielectric material are nickel, iron, nickel-iron alloy, and magnetic oxide.

The embodiment of the invention's transformer described in relation to FIGS. 1, 2A, 2B, and 2C achieves a small size relative to any known transformer in the art. One reason for achieving a small size is that through increasing the permeability of one or more of the dielectric layers 160, 162, or 164, higher inductance values for the primary and secondary windings of the invention's transformer are achieved. Moreover, because of the increase in the permeability of one or more of the dielectric layers 160, 162, or 164, the coupling coefficient between the invention's transformer's primary and second windings is also increased. The higher inductance and coupling coefficient values thus achieved in turn result in a more efficient transformer that occupies a much smaller area relative to any off-chip transformer. The small size of the invention's transformer makes possible the on-chip fabrication of the transformer which, as stated above, was previously unknown in the art.

One advantage of the small size of the present invention's on-chip transformer is that it can meet the need for decreasing electronic circuit component sizes and geometries. Moreover, another advantage of on-chip fabrication of the present embodiment of the invention's transformer is its long-term reliability. The interconnects of on-chip the invention's transformer are not subject to long-term damage from vibration, corrosion, chemical contamination, oxidation, and other chemical and physical forces because they are not exposed to those elements, but are inside the semiconductor chip.

The on-chip fabrication of the present invention's transformer is also cost-effective, since its fabrication can be easily assimilated into a process that is well known in the art, such as a CMOS process flow. The present embodiment of the invention's transformer does not require independent fabrication or assembly, as required by off-chip transformers. Also, the on-chip interconnect lines used for connecting to the present embodiment's transformer are extremely short compared to off-chip wires and off-chip interconnect lines that are necessary for connecting to off-chip transformers. As a result, the interconnect lines used for connecting various devices to the invention's transformer have very little unwanted resistance, capacitance, and inductance.

Further, the present embodiment of the invention's transformer benefits from the high quality factor of its inductors. As stated above, quality factor ("Q") of an inductor is proportional to its inductance, since the quality factor of an inductor is determined by Q=L/R, where L is the inductance and R is the resistance inherent in the inductor. Also, it is well known in the art that the inductance of an inductor is proportional to the permeability of the materials through which the magnetic field flux lines traverse. Since the permeability in any of dielectric layers 160, 162, or 164 is significantly increased through the various methods described above, the inductance of the invention's transformer's inductors and, therefore, the quality factors of those inductors, is also increased significantly.

Another exemplary embodiment of the present invention's transformer is shown in FIG. 3. FIG. 3 shows a top view of the invention's transformer 300 in this exemplary embodiment. The dielectric layer in which the invention's transformer 300 is fabricated is referred to by numeral 302 in FIG. 3. The primary winding of the invention's transformer 300, also called a "first conductor" in the present application, is referred to by numeral 304 in FIG. 3. The secondary winding of the invention's transformer 300, also called a "second conductor" in the present application, is referred to by numeral 306 in FIG. 3. It is noted that for primary winding 304 and second winding 306, a connection to the "inside" terminals, i.e. the terminals at the respective centers of the windings, can be made by tapping into the inside terminals from a metal layer above or below the metal layer in which primary winding 304 and secondary winding 306 are fabricated. Moreover, a connection to the "outside" terminal of secondary winding 306 can be made by tapping into the outside terminal from a metal layer above or below the layer in which primary winding 304 and secondary winding 306 are fabricated. However, a connection to the "outside" terminal of primary winding 304 is typically made by using metal interconnect in the same metal layer in which primary winding 304 and secondary winding 306 are fabricated. Dielectric layer 302 in FIG. 3 can comprise silicon dioxide, or a low-k dielectric such as porous silica, fluorinated amorphous carbon, fluoro-polymer, parylene, polyarylene ether, silsesquioxane; fluorinated silicon dioxide, and diamondlike carbon.

In the present embodiment's transformer 300 in FIG. 3, primary winding 304 and secondary winding 306 may be patterned within dielectric layer 302 by either a damascene process or by a subtractive etching process. Both the damascene process and the subtractive etching process are well known in the art and were briefly described in the exemplary embodiment of the invention's transformer in relation to FIGS. 1, 2A, 2B, and 2C.

It is noted that one difference between the embodiment of the invention's transformer in FIG. 3 and the embodiment of the invention's transformer in FIGS. 1, 2A, 2B, and 2C is that in the embodiment of the invention's transformer in FIG. 3, all interconnect metal segments belong to the same metallization level and as such are patterned in the same dielectric layer, i.e. dielectric layer 302. In contrast, in the embodiment of the invention described in FIGS. 1, 2A, 2B, and 2C, the various interconnect metal segments of the primary and secondary windings in the transformer were distributed in two different metallization levels and were interconnected by means of vias. Thus, while a number of interconnect metal segments were patterned in dielectric layer 260 in FIGS. 2A, 2B, and 2C, other interconnect metal segments were patterned in dielectric layer 264 in FIGS. 2B and 2C. For example, if interconnect metal segments in dielectric layer 260 are made in metallization level three, the interconnect metal segments in dielectric layer 264 are made in metallization level two.

The permeability of dielectric layer 302 in FIG. 3 may be increased by introducing into dielectric layer 302 atoms and/or molecules of high permeability materials through the techniques of implantation or ion sputtering. The permeability of dielectric layer 302 may also be increased by any of the other methods described in the exemplary embodiment of the invention's transformer in relation to FIGS. 1, 2A, 2B, and 2C. The present invention's transformer 300 achieves the same advantages of small size, high quality factor inductor windings, reliability, cost-effectiveness, and elimination of the requirement of connections through off-chip wires or off-chip interconnect lines, described in the exemplary embodiment of the present invention's transformer in FIGS. 1, 2A, 2B, and 2C.

Yet another exemplary embodiment of the present invention's transformer is shown in FIG. 4. FIG. 4 shows a perspective view of the invention's transformer 400. The primary winding of the invention's transformer 400, also called a "first conductor" in the present application, is referred to by numeral 408 in FIG. 4. The secondary winding of the invention's transformer 400, also called a "second conductor" in the present application, is referred to by numeral 410 in FIG. 4. The dielectric layer of the invention's

transformer 400 in FIG. 4 in which primary winding 408 is patterned is referred to by numeral 402. The dielectric layer of the invention's transformer 400 in FIG. 4 in which secondary winding 410 is patterned in is referred to by numeral 406. The dielectric layer of the invention's transformer 400 in FIG. 4 that is between dielectric layer 402 and dielectric layer 406 is referred to by numeral 404. For illustration purposes, primary winding 408 of transformer 400 in FIG. 4 is shown larger than secondary winding 410, and not directly under secondary winding 410. However, in the exemplary embodiment of the present invention's transformer 400 in FIG. 4, primary winding 408 can be directly under secondary winding 410 and can be of the same size as secondary winding 410. In the present invention's transformer 400 in FIG. 4, dielectric layers 402, 404, and 406 can comprise silicon dioxide, or any of the low-k dielectrics mentioned in the exemplary embodiment of the present invention's transformer in FIGS. 1, 2A, 2B, and 2C.

As in the prior exemplary embodiments of the present invention, the permeability in any of the dielectric layers 402, 404, or 406 in FIG. 4, or in a combination of any two of the dielectric layers, or in all three of the dielectric layers, may be increased by introducing into any of the dielectric layers 402, 404, or 406 atoms and/or molecules of high permeability materials through the method of implantation or ion sputtering. The permeability of dielectric layer 402, 404, or 406 may also be increased by any of the other methods described in the first exemplary embodiment of the invention's transformer in FIGS. 1, 2A, 2B, and 2C.

A difference between the present embodiment of the invention's transformer and the embodiment of the invention's transformer discussed in relation to FIGS. 1, 2A, 2B, and 2C is that in the present embodiment the entire primary winding is patterned in a single dielectric layer while the entire secondary winding is also patterned in a single, but a separate, dielectric layer. In other words, each of the primary and secondary windings are fabricated in their own separate dielectric layers. In contrast, in the embodiment of the invention's transformer shown described in relation to FIGS. 1, 2A, 2B, and 2C, the primary winding is distributed within three dielectric layers, i.e. dielectric layers 160, 162, and 164 as shown in FIG. 1. Likewise, the secondary winding is also distributed within the same three dielectric layers, i.e. dielectric layers 160, 162, and 164 as shown in FIG. 1.

A difference between the embodiment of the invention's transformer shown in FIG. 4 and the embodiment of the invention's transformer shown in FIG. 3 is that in the embodiment of the invention shown in FIG. 4, the entire primary winding is patterned in a single dielectric layer while the entire secondary winding is also patterned in a single, but a separate, dielectric layer. In other words, each of the primary and secondary windings are fabricated in their own separate dielectric layers. In contrast, in the embodiment of the invention shown in FIG. 3, both the primary winding and the secondary winding of the invention's transformer are patterned in a single, and the same, dielectric layer.

It is noted that the exemplary embodiment of the present invention's transformer 400 in FIG. 4 also achieves the advantages of small size, high quality factor inductor windings, reliability, cost-effectiveness, and elimination of the requirement of connections through off-chip wires or off-chip interconnect lines, as described in the first exemplary embodiment of the present invention's transformer in FIGS. 1, 2A, 2B, and 2C.

While certain embodiments of the invention are illustrated in the drawings and are described herein, it is apparent to

those of ordinary skill in the art that the specific embodiments described herein may be modified without departing from the inventive concepts described. For example, various combinations of materials may be used in various dielectric layers, examples of which are low dielectric constant materials such as porous silica, fluorinated amorphous carbon, fluoro-polymer, parylene, polyarylene ether, silsesquioxane, fluorinated silicon dioxide, and diamondlike carbon, to meet certain design requirements. In addition, various combinations of techniques known in the art may be used to accomplish the invention's concepts described herein.

Thus, on-chip transformers have been described.

What is claimed is:

1. A structure in a semiconductor chip, said structure comprising:

a dielectric area having a first permeability;

a permeability conversion material having a second permeability, said permeability conversion material being interspersed within said dielectric area, wherein said second permeability is greater than said first permeability;

a first conductor patterned into said dielectric area, said first conductor having a first plurality of turns;

a second conductor patterned into said dielectric area, said second conductor having a second plurality of turns.

2. The structure of claim 1 wherein said dielectric area comprises at least three dielectric layers.

3. The structure of claim 1 wherein said dielectric area comprises a plurality of dielectric layers, wherein said first conductor is in a first dielectric layer of said plurality of dielectric layers, wherein said second conductor is in a third dielectric layer of said plurality of dielectric layers, and wherein a second dielectric layer of said plurality of dielectric layers is situated between said first and third dielectric layers.

4. The structure of claim 3 wherein said plurality of dielectric layers comprise a low-k dielectric.

5. The structure of claim 3 wherein said plurality of dielectric layers comprise silicon dioxide.

6. The structure of claim 1 wherein said dielectric area comprises a low-k dielectric.

7. The structure of claim 1 wherein said permeability conversion material is selected from the group consisting of nickel, iron, nickel-iron alloy, and magnetic oxide.

8. The structure of claim 1 wherein said dielectric area comprises silicon dioxide.

9. The structure of claim 1 wherein said first conductor is selected from the group consisting of copper, aluminum, and copper-aluminum alloy.

10. The structure of claim 1 wherein said second conductor is selected from the group consisting of copper, aluminum, and copper-aluminum alloy.

11. A structure in a semiconductor chip, said structure comprising:

a first dielectric layer;

a second dielectric layer situated over said first dielectric layer, said second dielectric layer being interspersed with a permeability conversion material;

a third dielectric layer situated over said second dielectric layer;

a primary winding patterned into said first, second, and third dielectric layers;

a second winding patterned into said first, second, and third dielectric layer.

12. The structure of claim 11 wherein said primary winding comprises a plurality of interconnect metal segments in said first dielectric layer and a plurality of interconnect metal segments in said third dielectric layer.

13. The structure of claim 12 wherein a plurality of via metal segments in said second dielectric layer interconnect said plurality of interconnect metal segments in said first dielectric layer with said plurality of interconnect metal segments in said third dielectric layer.

14. The structure of claim 11 wherein said secondary winding comprises a plurality of interconnect metal segments in said first dielectric layer and a plurality of interconnect metal segments in said third dielectric layer.

15. The structure of claim 14 wherein a plurality of via metal segments in said second dielectric layer interconnect

said plurality of interconnect metal segments in said first dielectric layer with said plurality of interconnect metal segments in said third dielectric layer.

16. The structure of claim 11 wherein said first dielectric layer is interspersed with a permeability conversion material.

17. The structure of claim 11 wherein said third dielectric layer is interspersed with a permeability conversion material.

18. The structure of claim 11 wherein said first and said third dielectric layers are interspersed with a permeability conversion material.

19. The structure of claim 11 wherein said permeability conversion material is selected from the group consisting of nickel, iron, nickel-iron alloy, and magnetic oxide.

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